ICL5102

Resonant Controller IC 2nd Generation with PFC for Power Supply and Lighting Drivers

Datasheet

Rev. V1.0, 2017-06-09

Power Management & Multimarket

Resonant Controller IC with PFC for Power Supply and Lighting Drivers

Product highlights

- Integrated PFC and HB controllers
- Supports universal input (70V_{AC} to 325V_{AC}) and wide output range
- Low count of external components supporting small form factors and a cost efficient design
- All parameters set by simple resistors only
- Junction temperature Range -40 °C to +125 °C
- Comprehensive set of protection features
- Fast startup < 500 ms, $I_{Startup}$ < 100µA
- Power Factor Correction > 99 %, THD < 5 %
- High efficiency up to 94 %
- Active BURST Mode for low Standby < 300mW with Enable / Disable function supports dimming

PFC controller features

- 3 State Self-adapting Soft Start for soft on
- Brownout Detection
- Boundary mode operation during nominal load and WCM mode during low load down to 0.1 %
- Improved THD compensation
- Adjustable PFC current limitation

Resonant HB controller features

- Fully integrated 650 V high-side driver
- Self-adaptive dead time 250ns – 750ns
- Detection of capacitive operation, overload, short circuit, output over voltage OVP & hot spot over temperature via NTC, Surge protection using in all cases Auto Restart
- Adjustable Frequency 20kHz / 325kHz / 1.3MHz

PG-DSO-16

Applications

- Offline AC-DC Power Supply, LCD TV, Adapter
- LED driver, e.g. commercial or residential lighting systems > 50 W
- Integrated electronic control gear for LED luminaires

Description

The Resonant controller ICL5102 is designed to control resonant converter topologies. The PFC stage operates in Boundary Mode and WCM mode, supporting low load conditions. Integrated high and low side drivers assure a low count of external components, enabling small form factor designs.
ICL5102 parameters are adjusted by simple resistors only, this being the ideal choice to ease the design-in process. A comprehensive set of protection features using Auto Restart ensures that the controller detects fault conditions, protecting both drivers and load. Figure 1 shows a typical application.

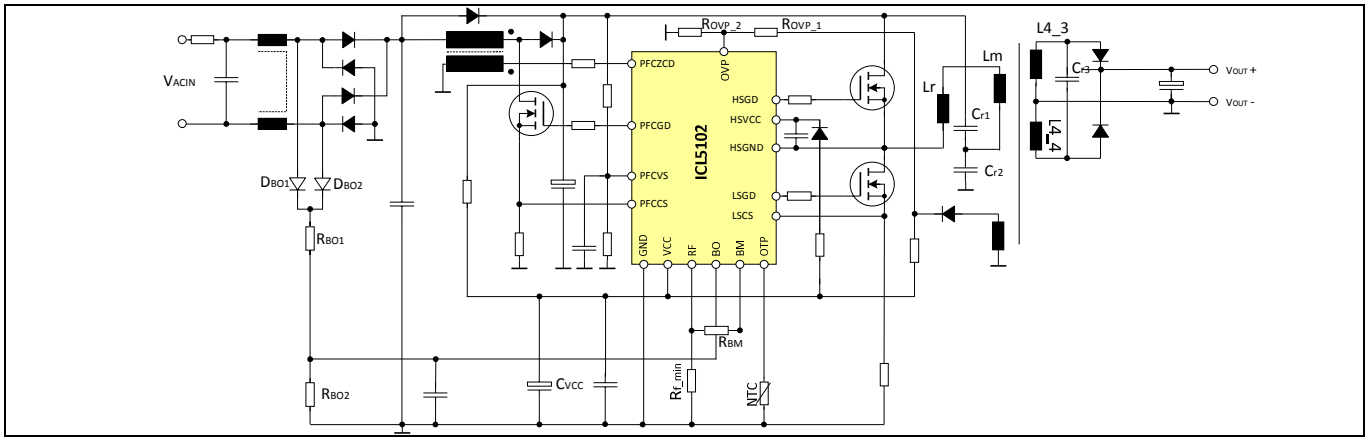

Figure 1 Generic LCC Application

Product type	Package
ICL5102	PG-DSO-16

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1 Pin Configuration and Description

The pin configuration is shown in Figure 2 PG-DSO-16 Package

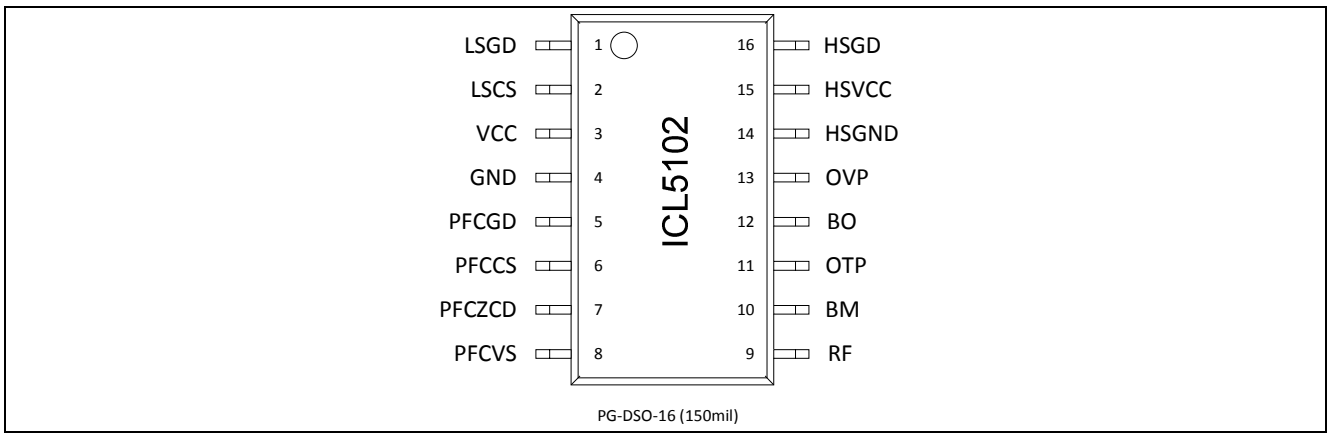

Figure 2. Pin Configuration

1.1 PIN Configuration for PG-DSO-16

Symbol	Pin	Function
LSGD	1	Low-side gate drive
LSCS	2	Low-side current sense signal
VCC	3	Low-side chip supply voltage
GND	4	IC GND
PFCGD	5	PFC gate drive
PFCCS	6	PFC current sense signal
PFCZCD	7	PFC zero crossing detection
PFCVS	8	PFC voltage sensing
RF	9	RUN frequency setting
BM	10	Burst mode setting
OTP	11	Over Temperature protection
BO	12	Brown out detection
OVP	13	Overvoltage protection
HSGND	14	High-side GND
HSVCC	15	High-side supply voltage
HSGD	16	High-side gate drive

1.2 PIN Set-Up

The PIN set-up of ICL5102 for a typical PFC / LLC converter is shown in Figure 3.

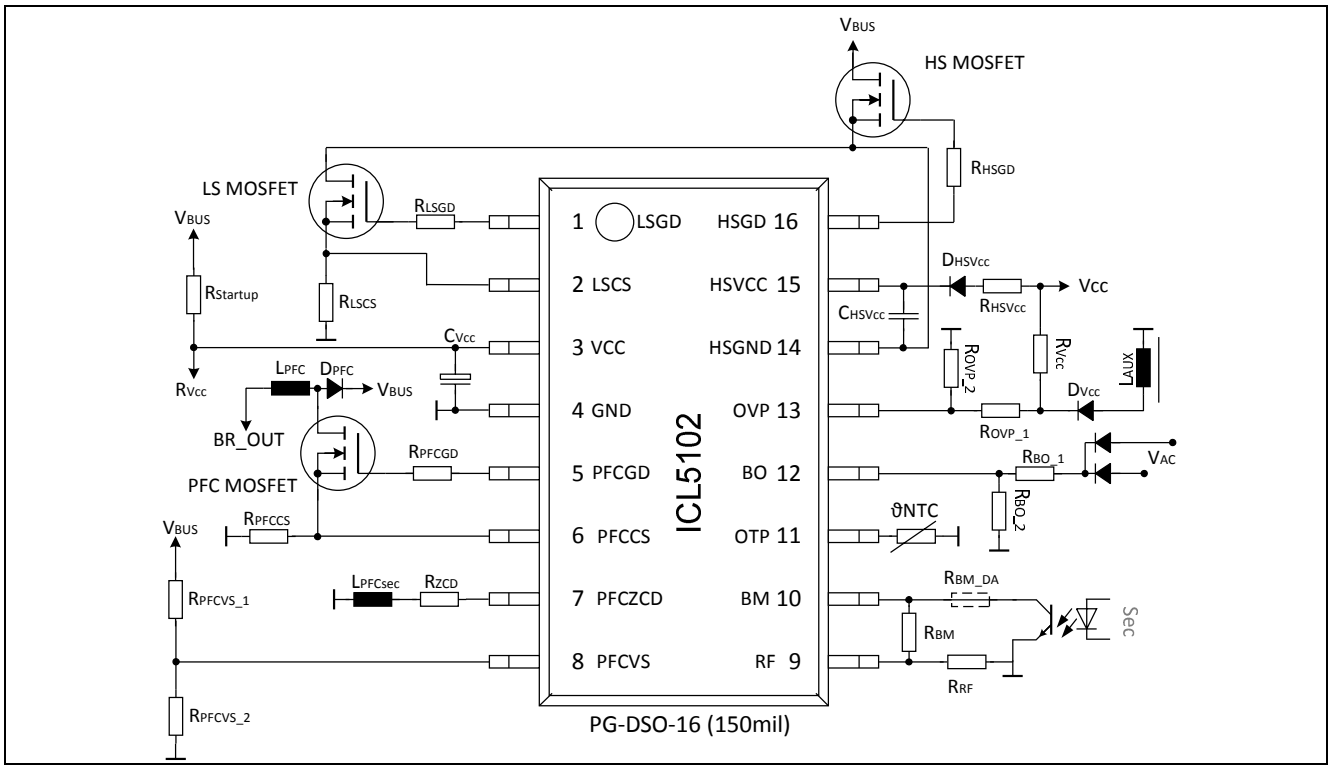

Figure 3 PIN Set-Up

1.3 PIN Functionality

Table 1. Pin Definitions and Functions

Symbol	Pin	Function
LSGD	1	**Low-Side Gate Drive** The gate of the low-side MOSFET in a resonant inverter topology is controlled by this pin. There is an active L-level during UVLO (under voltage lockout) and a limitation of the max H-level at 11.0 V during normal operation. In order to turn on the MOSFET softly (with a reduced di_{DRAIN}/dt), the gate voltage rises typically within 245 ns from L-level to H-level. The fall time of the gate voltage is less than 50 ns in order to turn off quickly. This measure produces different switching speeds during turn-on and turn-off as it is usually achieved with a diode parallel to a resistor in the gate drive loop. It is recommended to use a resistor of typically 10 Ω between the drive pin and gate in order to avoid oscillations and in order to shift the power dissipation when discharging the gate capacitance into this resistor. The dead time between the LSGD signal and HSGD signal is self-adapting between 250 ns and 750 ns.
LSCS	2	**Low-Side Current Sense Signal** This pin is connected via a serial resistor to the shunt, which is located between the source terminal of the low-side MOSFET of the inverter and ground. Internal clamping structures and filtering measures allow sensing of the source current for the low side inverter MOSFET without additional filter components. There is a first threshold of 0.8 V sensed by each ½ cycle. If this threshold is reached, the over current control increases the frequency until the signal is below 0.8V. If the sensed current signal exceeds a second threshold of 1.6 V for longer than 500 ns, the IC stops the half bridge MOSFETs. If this signal is present for longer than 5µs, the controller powers down and auto restarts the system. There are further thresholds active at this pin that detect a capacitive mode operation. A voltage level below -50 mV before the high-side gate is on indicates faulty operation (operation below resonance). The 1.6V threshold senses even short over currents during turn-on of the high-side MOSFET as typical for reverse recovery currents of a diode. If one of these comparator thresholds indicates incorrect operating conditions for longer than 620 µs the IC turns off the gates and changes to fault mode due to detected capacitive mode operation (non-zero voltage switching). The threshold of -50mV is also used to adjust the dead time between turn-off and turn-on of the resonant drivers in a range of 250 ns to 750 ns during all operating modes. The capacitive load regulation will be active if the threshold of +50 mV is reached within a time of 6% of the period time. In order to prevent a capacitive load operation, the controller increases the frequency until the area of capacitive load is left.

VCC	3	**Low-Side Chip Supply Voltage** This pin provides the power supply of the ground-related section of the IC. There is a turn-on threshold at typ. 16.0 V and an UVLO threshold at typ. 9.0 V. The upper supply voltage limit is 17.5 V ($V_{CCabsmax}$ = 18.5V). There is an internal Zener diode clamping V_{CC} at 16.3 V (at I_{VCC} = 2 mA typically). The maximum Zener current is internally limited to 5 mA. An external Zener diode is required for higher current levels. Current consumption during UVLO and during fault mode is less than typ. 80 µA. A ceramic capacitor close to the supply and GND pin is required in order to act as a low-impedance power source for gate drive and logic signal currents. Note, the clamping is only active after shut ON. This ensures a safe start up.
GND	4	**IC GND** This pin is connected to ground and represents the ground level of the IC for the supply voltage, gate drive and sense signals.
PFCGD	5	**PFC Gate Drive** The gate of the MOSFET in the PFC pre-converter designed in boost topology is controlled by this pin. There is an active L-level during UVLO and a limitation of the max H-level at 11.0 V during normal operation. In order to turn on the MOSFET softly (with a reduced di_{DRAIN}/dt), the gate drive voltage rises within 245 ns from L-level to H-level. The fall time of the gate voltage is less than 50 ns in order to turn off quickly. A resistor of typically 10 Ω is recommended between the drive pin and gate in order to avoid oscillations and in order to shift the power dissipation when discharging the gate capacitance into this resistor. The PFC section of the IC controls a boost converter as a PFC pre-converter in discontinuous conduction mode (DCM). Typically, the control starts with an initial ON Time depending on the line input voltage sensed by the BO PIN. Gate drive pulses with a fixed on-time of typically 6.0 µs at V_{BO} = 2.0 V, increasing up to 24 µs and with an off-time of 47 µs. As soon as sufficient zero current detector (ZCD) signals are available, the operation mode changes from fixed frequency operation to operation with variable frequency. The PFC works in critical conduction mode operation (CrCM) when rated and/or medium load conditions are present. That means triangular-shaped currents in the boost converter choke without gaps and variable operating frequency. During very low load the operation mode switches to discontinuous conduction mode (DCM) – that means triangular-shaped currents in the boost converter choke with gaps when reaching the zero current level and variable operating frequency in order to avoid steps in the consumed line current. During initial start-up and Burst Mode, the ON time of the PFC is for 10µs fixed to 2.5µs. After 10µs the Brown Out voltages set the ON time depending on the line input voltage.
PFCCS	6	**PFC Current Sense Signal** The voltage drop across a shunt resistor located between the source of the PFC MOSFET and GND is sensed with this pin. If the level exceeds a threshold of 1.0 V for longer than 200 ns, the PFC gate drive is turned off until the zero current detector (ZCD) enables a new cycle.

PFCZCD	7	**PFC Zero Crossing Detection** This pin senses the current through the boost inductor. If this current becomes zero during the off-time of the PFC MOSFET, the controller initiates a new cycle. A resistor connected between the ZCD winding and PIN 7 limits the sink and source current of the sense pin when the voltage of the ZCD winding exceeds the internal clamping levels (typically 6.3 V and -2.9 V @ 5 mA) of the IC. If the sensed voltage level of the ZCD winding is not sufficient (e.g. during start-up), an internal start-up timer will initiate a new cycle every 52 µs after the turn-off of the PFC gate drive. The clamping current out of this pin during the on-time of the PFC MOSFET indicates the voltage level of the AC supply voltage. During low input voltage levels, the on-time of the PFC MOSFET is enlarged in order to minimize gaps in the line current during zero crossing of the line voltage and improve the THD (Total Harmonic Distortion) of the line current. Optimization of the THD is possible by trimming of the resistor between this pin and the ZCD winding to adapt the THD correction to the inductance and PFC MOSFET. If no ZCD signal is available within 52 µs after turn-off of the PFC gate drive, a new cycle is initiated through an internal start-up timer.
PFCVS	8	**PFC Voltage Sensing** The intermediate circuit voltage (bus voltage) at the smoothing capacitor is sensed by a resistive divider at this pin. The internal reference voltage for the rated bus voltage is 2.5 V. There are further thresholds at < 12.5 % of the rated bus voltage for detection of open control loop, < 75 % for detection of under voltage during start up. An over voltage is detected during power up if Vbus is > 105 %, > 109 % and > 115 %. The over voltage threshold operates with a hysteresis of 100mV (4 % of the rated bus voltage). It is recommended to use a small capacitor between this pin and GND as a spike suppression filter. In run mode, PFC over voltage stops the PFC gate drive within 5 µs. As soon as the bus voltage is less than 105 % of the rated level, the gate drives are enabled again. If the PFC over voltage 115 % lasts for longer than 50 ms, an inverter over voltage is detected and turns off the inverter gate drives, too.
RF	9	**Set minimum RUN Frequency** A resistor from this pin to ground sets the minimum operating frequency of the LLC / LCC inverter. This frequency limits the maximum output power. The combination of RRF and RBM sets the nominal frequency. This frequency must be lower than the expected run frequency during nominal load condition. The run frequency range is 20 kHz to 325 kHz. How to calculate the resistors see chapter 2.2.
BM	10	**Burst Mode** In order to achieve very low standby power consumption, the ICL5102 has an integrated active burst mode. Active means that the IC senses the status of the output stage and reacts. A resistor from pin 10 (BM) to RF (PIN 9) sets the operating frequency range of the LLC / LCC converter depending on the load. Furthermore, it is possible to enable the BURST MODE function at a certain level or disable burst mode. How to calculate the resistor R_{BM} see chapter 2.2.

OTP	11	**Over Temperature Protection** The Over Temperature protection detects the temperature of an external NTC temperature sensor located on the PCB. In case of using OTP, use a parallel capacitor to the NTC to GND of max. 100pF. If this function is not in use, a 20k resistance can be connected from PIN 11 to GND. NOTE: If OTP is disabled, do NOT set a capacitor parallel to the 20k resistor to GND. This prevents a malfunction during Burst Mode. For external OTP use an NTC from PIN 11 to GND. If the voltage V_{OTP1} is < 703mV during start-up, the controller prevents a power up. If the voltage at pin 11 drops below V_{OTP2} < 625mV during RUN or Burst Mode, the IC powers down and auto restarts when V_{OTP} > 703mV. Delay in both cases is 620µs, the typical current at this pin is I_{OTP} = 100µA.
BO	12	**Brown out Detection** AC Line Input Voltage feedforward to set the initial pulse time for the PFC during the very first START UP and the max ON time – depending on the line input voltage. Furthermore, the brown out pin sets the fixed PFC gate pulse width during Burst Mode depending on line input voltage. The voltage at this pin must be above V_{BO} > 1.4V during monitoring to enable a brown in. If the voltage at this pin drops below V_{BO} < 1.2V for longer than 50ms during operation, a brown out is detected and the controller powers down and auto restarts the internal system. Use a double rectifier and high ohm resistors for the voltage devider.
OVP	13	**Over Voltage Protection** The ICL5102 has an integrated precise and fast reacting output overvoltage protection by sensing the secondary side output directly at the chip supply AUX winding after the rectifier diode. This protection can be enabled or disabled. If the voltage at this pin exceeds V_{OVP} > 2.5V for longer than 5µs during the start-up phase, the controller prevents a power up. In case the voltage at pin 13 exceeds during RUN or Burst Mode the V_{OVP} > 2.5V threshold for longer than 5µs, the IC powers down and restarts automatically. To disable this function, set this pin to IC GND.
HSGND	14	**High-Side GND** This pin is connected to the source terminal of the high-side MOSFET, which is also the output of the half bridge. This pin represents the floating ground level of the high-side driver and the high-side supply.
HSVCC	15	**High-Side Supply Voltage** This pin provides the power supply of the high-side section of the IC. An external capacitor between pins 14 and 15 acts as boot strap capacitor, which has to be recharged cycle by cycle via a high-voltage diode from the low-side supply voltage during the on-time of the low-side MOSFET. An UVLO threshold with hysteresis enables the high-side section at 10.4 V and disables it at 8.6 V.
HSGD	16	**High-Side Gate Drive** The gate of the high-side MOSFET in a resonant inverter topology is controlled by this pin. There is an active L-level during UVLO and a limitation of the max H-level at 11.0 V during normal operation. The switching characteristics are the same as described for LSGD (pin 1). It is recommended to use a resistor of about 10 Ω between the drive pin and gate in order to avoid oscillations and in order to shift the power dissipation when discharging the gate capacitance into this resistor. The dead time between the LSGD signal and HSGD signal is self-adapting between 250 ns and 750 ns (typically).

2 Feature Description

2.1 Soft Start

The soft start consists of 3 subsequent states within a total minimum duration of t < 7ms. The ICL5102 stays in each soft start state as long as the $V_{LSCSpeak}$ > 0.8V and continues to the next state when $V_{LSCSpeak}$ < 0.8V.

The initial soft start frequency at line voltage first ON or at auto restart is:

$$f_{SoftStart} = 4*(f_{MAX} - f_{MIN}) + f_{MIN}$$

Equation 1: Initial Soft Start Frequency

During state 1 the frequency drops down within 624µs as in the followed equation:

$$f_{SS\_1} = f_{MIN} + 2.6*(f_{MAX} - f_{MIN})$$

Equation 2 Soft Start Frequency in State 1

During state 2 the frequency ramps down to f_{MAX} within 2.5ms

$$f_{SS\_2} = f_{MAX}$$

Equation 3: Soft Start Frequency in State 2

During state 3 the frequency ramps down to f_{MIN} within 3.75ms

$$f_{SS\_3} = f_{MIN}$$

Equation 4: Soft Start Frequency in State 3

During state 1 and 2, the voltage at the BM pin is driven internally to V_{BM} = 0.75V. During state 3, the voltage at the BM pin ramps up from 0.75V up to 2.25V.

During soft start the voltage at the BM pin is driven by an internal ramp generator. This ramp generator can only sink current. Once the external opto-coupler takes away all current through the R_{BM} resistor from the ramp generator the soft start ends.

The operational range for the maximum initial soft start frequency f_{InSS} is 1300kHz. As it has a fixed relation to f_{MAX}-f_{MIN} the maximum soft start frequency may limit the maximum operation frequency f_{MAX} to less than 325kHz.

2.2 Frequency Setting

A Resonant Converter changes the frequency from a given minimum frequency $\mathbf{f_{min}}$ (full load, maximum power delivery) to a certain maximum frequency $\mathbf{f_{max}}$ that is reached at light load. The minimum frequency has to be chosen such that the converter doesn't enter capacitive switching under any load condition. The maximum frequency must not be too high in order to reduce switching losses and not compromise EMI.

In ICL5102 PIN RF delivers a constant voltage of V_{RF} = 2.5V. The current out of this pin defines the operating frequency, with a frequency to current ratio C_{FC} (typically $3.8*10^8$ Hz/A). PIN BM is clamped to V_{BMmax} = 2.25V. The minimum and maximum frequencies f_{min} and f_{max} are set by the resistors R_{RF} and R_{BM} shown in the block diagram on the left.

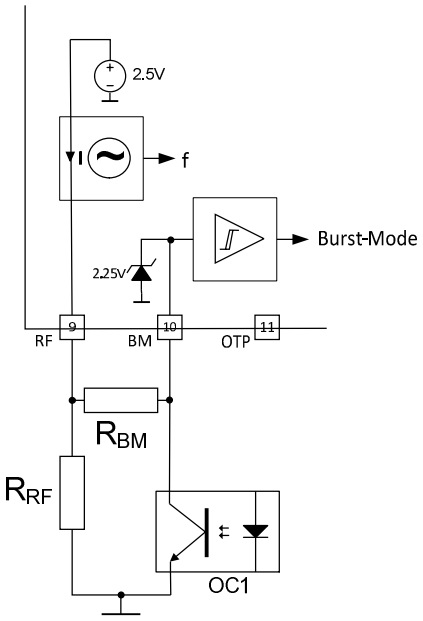

Figure 4 Generic Frequency / Burst Mode Block Diagram

Note:

If burst-mode is used, the maximum possible frequency range of ICL5102 in normal operation is:

$$f_{max} < 7 * f_{min}$$

Equation 5 Maximum Frequency

2.2.1 Minimum Frequency f_{MIN} @ maximum Load

f_{min} is reached when the collector current of opto-coupler OC1 is 0µA and the whole current through R_{BM} flows into PIN BM. That means $V_{BM} = V_{BMmax} = 2.25V$ in this operating point.

$$f_{\min} = C_{fc} * (I_{RF} + I_{RBM}) = C_{fc} * (\frac{2.5V}{R_{RF}} + \frac{2.5V - 2.25V}{R_{BM}})$$

Equation 6: Calculation of the minimum Frequency

2.2.2 Maximum Frequency f_{MAX} Before Entering Burst Mode

f_{max} is reached when the opto-coupler current is high enough to lower the voltage @ BM to 0.75V.

$$f_{\max} = C_{fc} * (I_{RF} + I_{RBM}) = C_{fc} * (\frac{2.5V}{R_{RF}} + \frac{2.5V - 0.75V}{R_{BM}})$$

Equation 7: Calculation of the maximum Frequency

2.2.3 Calculation of R_{RF} and R_{BM}

In order to determine the values for R_{RF} and R_{BM} the frequencies f_{min} and f_{max} must be defined as mentioned above. Equations I and II can then be solved for R_{BM} and R_{RF}:

$$R_{BM} = C_{fc} \frac{1.5V}{f_{\max} - f_{\min}} = 3.8 * 10^8 \frac{Hz}{A} * \frac{1.5V}{f_{\max} - f_{\min}}$$

$$R_{RF} = C_{fc} \frac{15V}{7 * f_{\min} - f_{\max}} = 3.8 * 10^8 \frac{Hz}{A} * \frac{15V}{7 * f_{\min} - f_{\max}}$$

Equation 8: Calculation of R_{BM} and R_{RF}

2.3 Burst Mode

2.3.1 Burst Mode Introduction

The ICL5102 burst mode concept is made for lowest standby power during dimming, no load conditions or µC use for STB < 500mW. The burst mode is self-adapting with an immediate response to load steps.

Dependent on the voltage at the BM PIN 10, the ICL5102 enters the Burst Mode, starts a burst pulse train, stops the pulse train or exits burst mode. Burst mode will be entered when the voltage at the BM PIN 10 drops below $V_{BMEnter}$ = 0.75V for at least 10ms. The block diagram bleow shows the internal functionality of the burst mode operation. In order to regulate the power during the burst pulse train, a serial resistor R_{PL} from PIN 2 LSCS to the shunt resistors can be adjusted experimental from 200Ω up to 1k depending on the application. Furthermore, a ceramic capacitor C_{Opto} at the opto-coupler should not exceed 1nF shown in Figure 5. Figure 6 shows the block diagram of the burst mode.

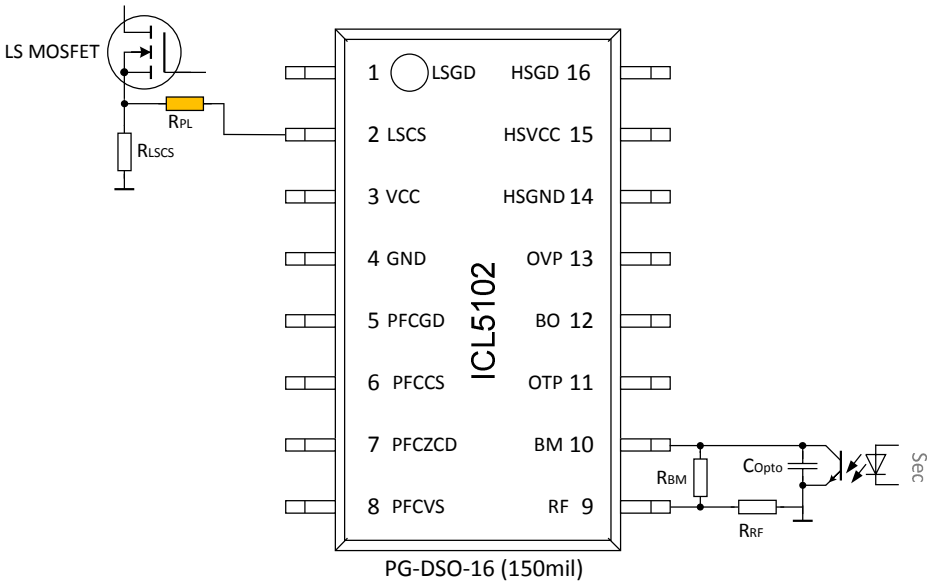

Figure 5 Power Limiting Resistor and Opto-coupler Capacitance

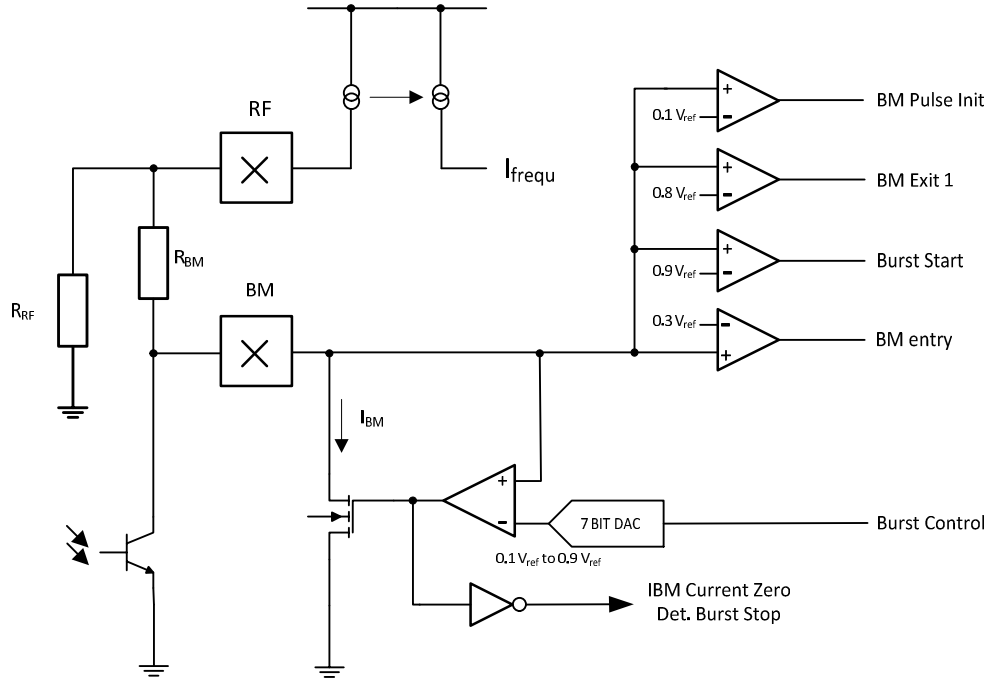

Figure 6 Burst Mode Block Diagram

2.3.2 Burst Mode Entry

The ICL5102 starts BM with a soft-off phase $f_{SoftOFF} \geq f_{max}$ in the first burst pause. During burst sleep all gate drives are off – the low side, high side and PFC gate.

$$f_{SoftOFF} = \frac{4}{3} * (f_{MAX} - f_{MIN}) + f_{MIN}$$

Equation 9: Calculation of the Soft OFF Frequency

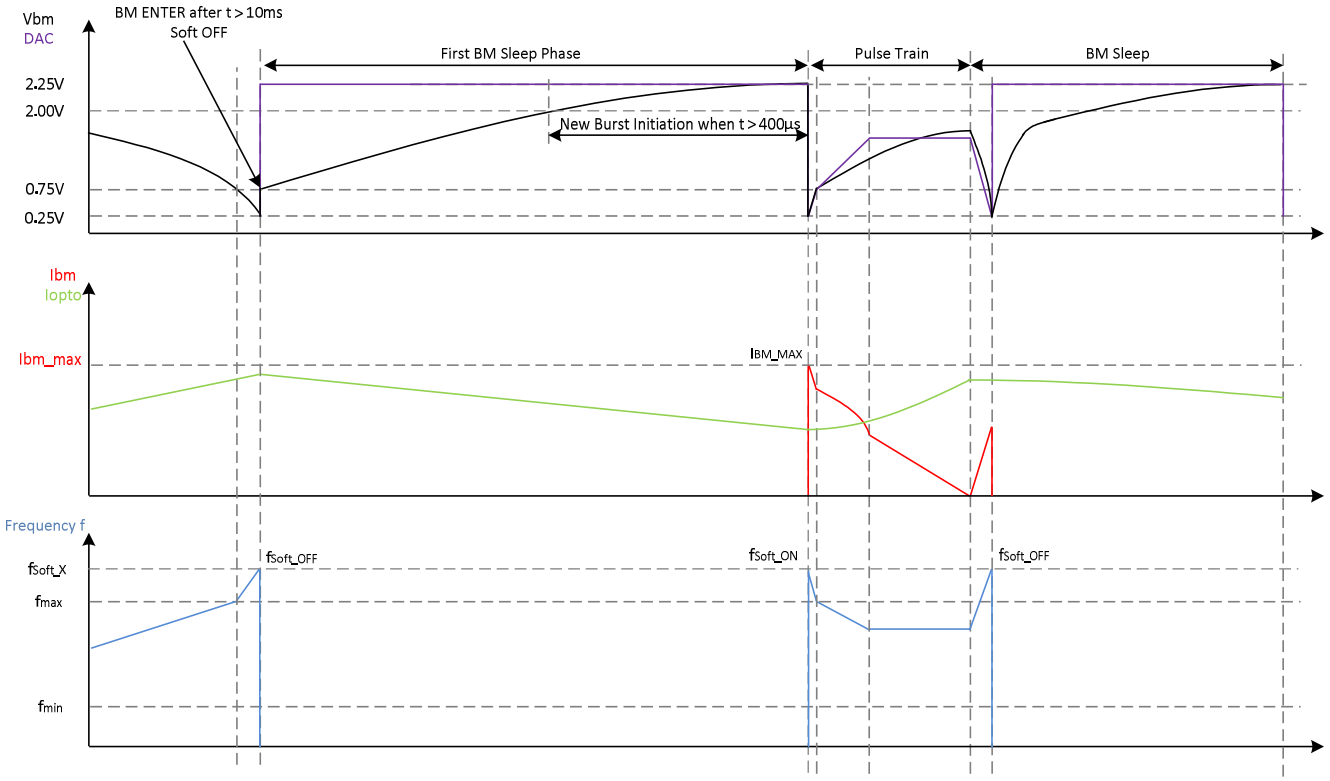

Figure 7: Burst Mode Entry

2.3.3 Burst ON (Pulse Train) – Voltage Mode Design

The burst pulse train starts with a higher frequency $f_{SoftON} > f_{max}$ in order to prevent noise or capacitive load operation. Determined by an internal counter, the frequency quickly ramps down to f_{max}. At the end of this ramp the frequency reaches a stable value determined by an internal power regulation loop. At the same time the current through the opto-coupler is monitored and when it reaches an internally defined value, a soft-off is initiated and the pulse train ends.

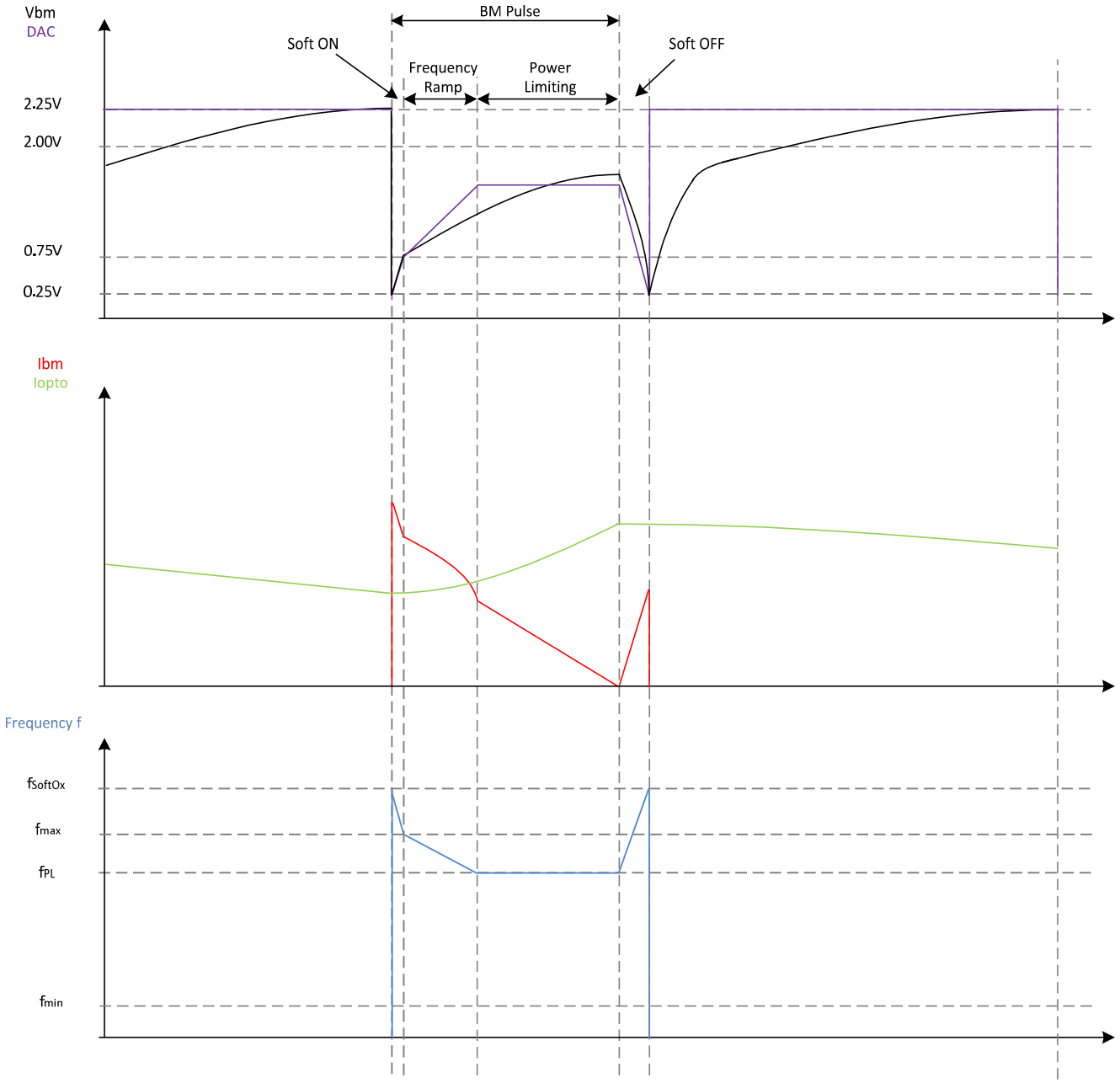

Figure 8: Pulse Train

2.3.4 Burst ON (Pulse Train) Phase I: SOFT ON (fixed)

Soft ON Start:

Soft ON will be activated when the voltage at the BM PIN drops to V_{BM} = 0.25V (the lowest voltage of the internal DAC). During Soft ON Start, the frequency is internally set to:

$$f_{SoftON} = \frac{4}{3} * (f_{MAX} - f_{MIN}) + f_{MIN}$$

Equation 10: Calculation of the Soft ON Frequency

The internal burst mode current I_{BM} is at the highest level: I_{BM_MAX}.

Soft ON Phase:

During Soft ON phase, the internal Counter of the DAC reduces the frequency f_{SoftON} down to f_{MAX} within 8 steps, each HB cycle (4LSB). Also the internal burst mode current decreases to a certain level.

Soft ON END

The end of soft on is initiated after 8 HB cycles, when the voltage at the BM PIN reaches V_{BM} = 0.75V.

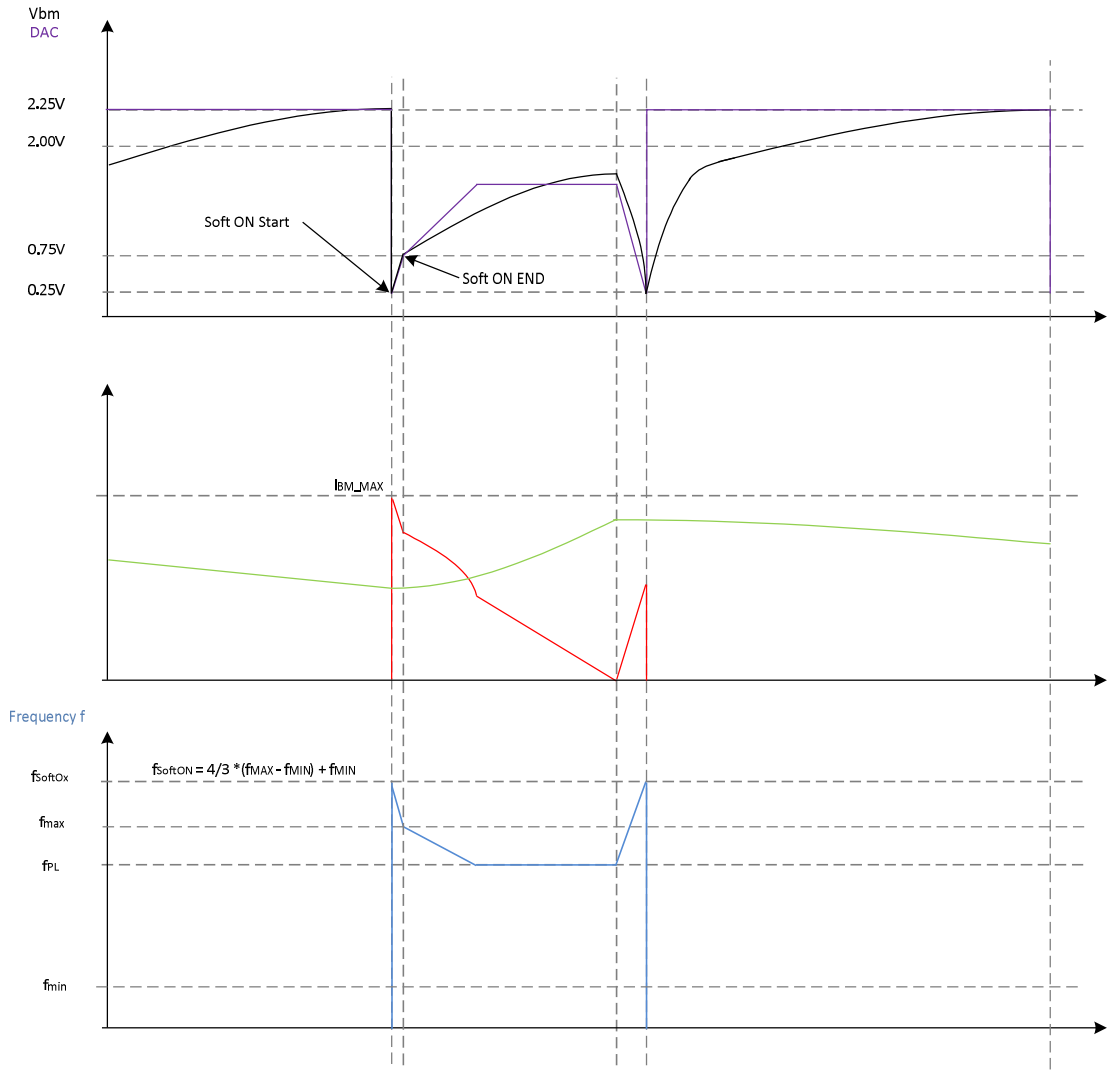

Figure 9: Pulse Train Soft ON

2.3.5 Burst ON (Pulse Train) Phase II: Frequency Ramp

The frequency reduces in order to reach the maximum power; the burst mode current I_{BM} decreases also from I_{BM_HIGH} to I_{BM}. Depending on an internal comparator result (see chapter 2.3.6), the frequency will be decreased with 4 LSB starting at f_{MAX} until the power limiter stops the frequency decrease and enters the next phase III (2.3.6).

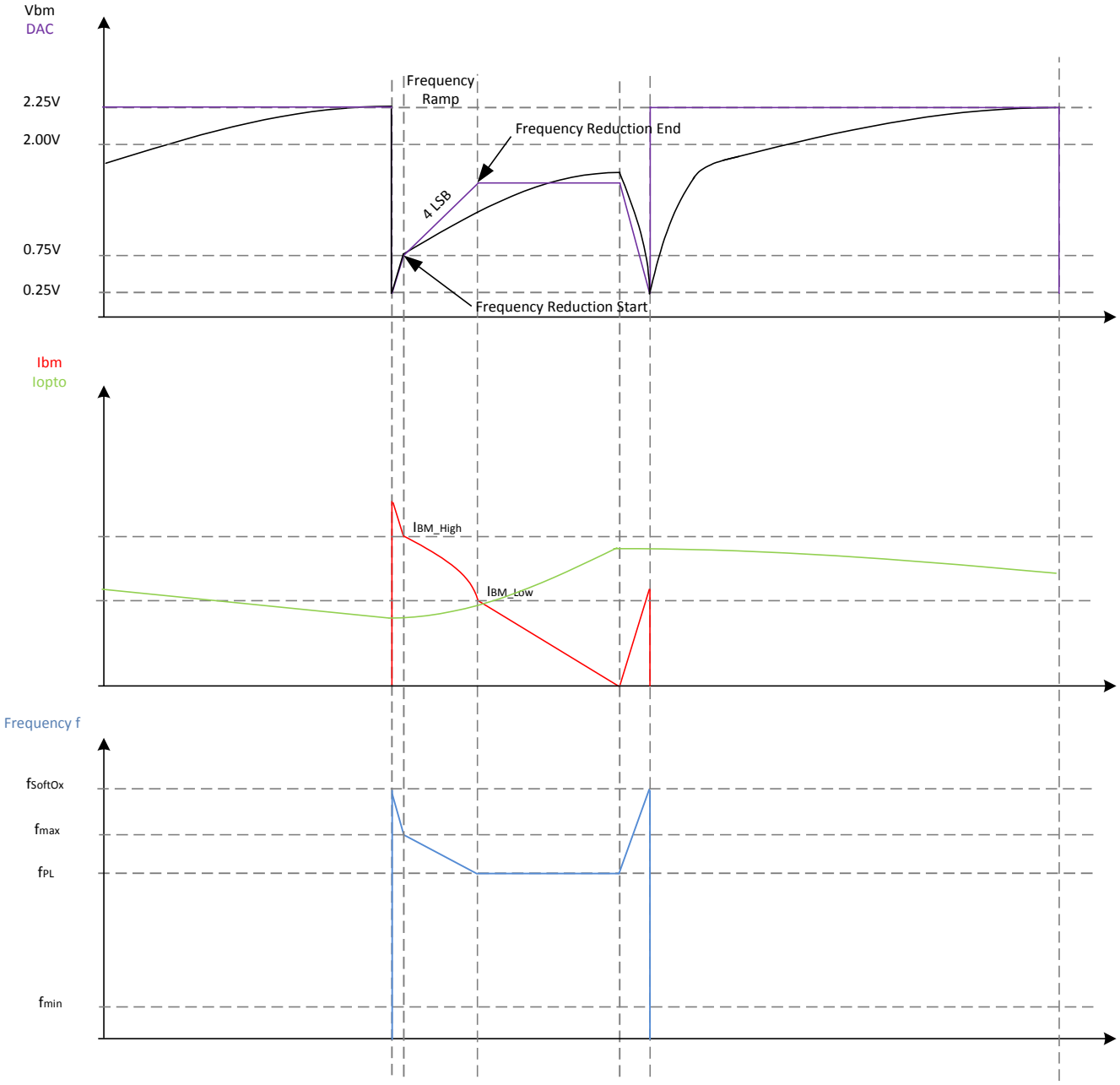

Figure 10: Pulse Train Frequency Ramp

2.3.6 Burst ON (Pulse Train) Phase III: Power Limitation

After adjusting the frequency to the max power in phase II, the controller will hold a constant frequency with a regulation of ± 1LSB depending on the comparator shown in 2.3.5. The opto-coupler current increases depending on the status of the output stage and the burst mode sink current decreases from I_{BM_Low} to I_{BM} = 0µA. In the moment of I_{BM} = 0µA, the power limitation phase / Pulse Train ends.

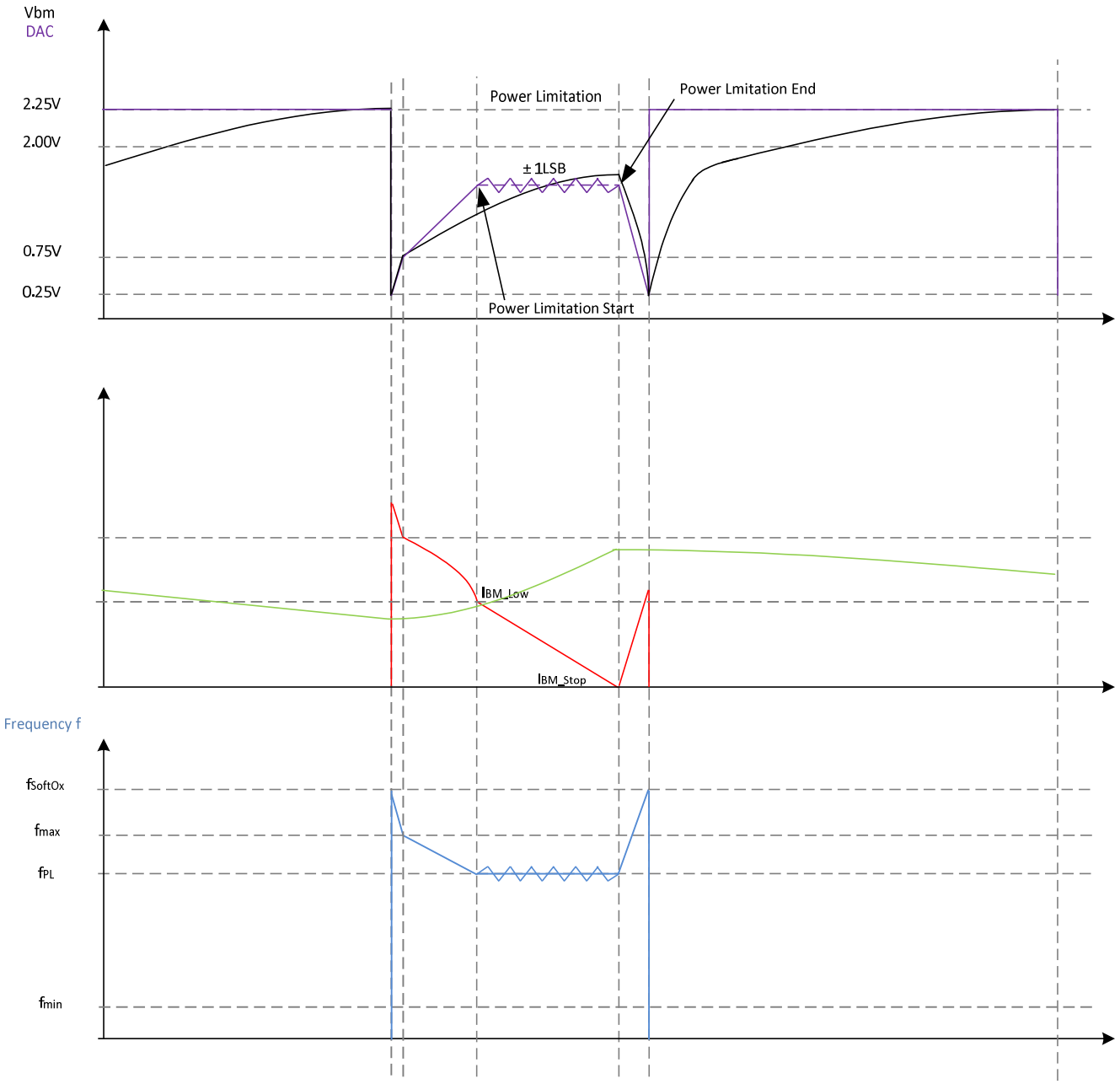

Figure 11: Pulse Train Frequency Ramp

In Phase III, a serial resistor (R_{PL} in orange below) from LSCS to the shunt will limits the power transfer during burst mode. The value of this resistor should be between R_{PL} = 200Ω and 1k.

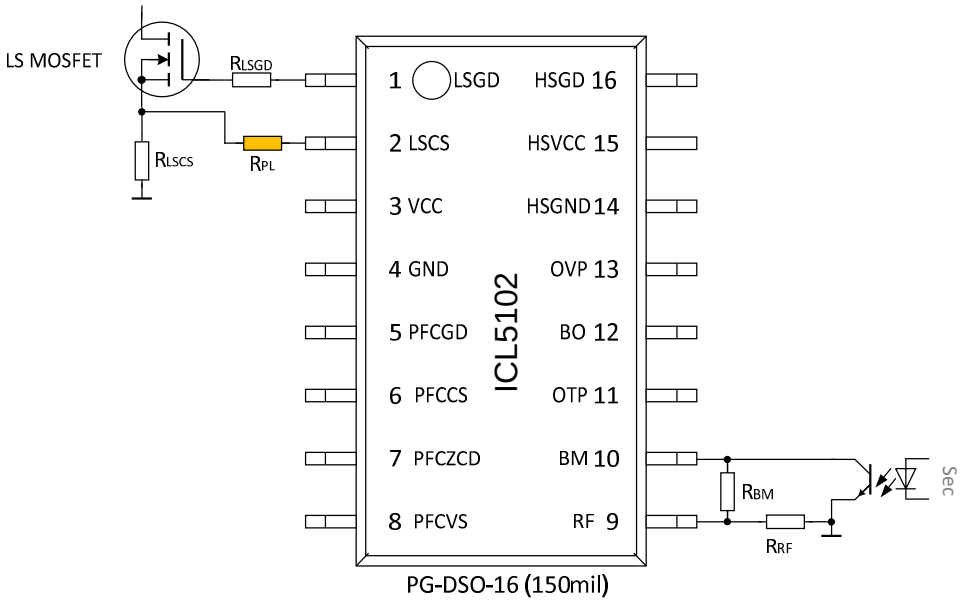

Figure 12: Power Limitation Resistance Setting R_{PL}

An internal power limitation is active. The threshold of the power limitation can be set by the value of R_{PL} as shown below. The voltage on the LSCS PIN will be integrated and compared internally with a 100µA signal.

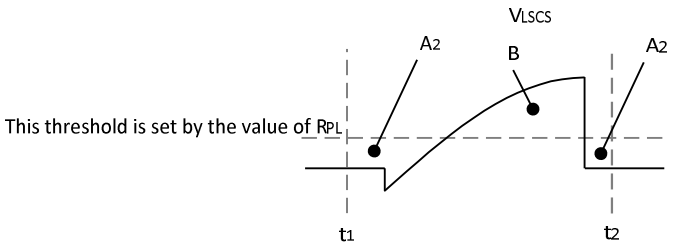

Figure 13: Low Side Current Sense Threshold for Power Limitation

If the integration of both areas A1 + A2 = B is ≠ zero the power limiter increases / decreases the frequency with 1LSB, the burst mode current I_{BM} varies.

2.4 Burst Mode EXIT

The ICL5102 Burst Mode Concept has 4 different EXIT conditions. ICL5102 differentiates between load steps during burst pulse, burst pause, timeout and duty cycle of burst pulse/pause.

2.4.1 EXIT 1: Load Step during Burst OFF (Sleep)

The condition of exit 1 is a voltage increase from V_{BM} = 2.0V up to V_{BM} = 2.25V within t < 400µs.

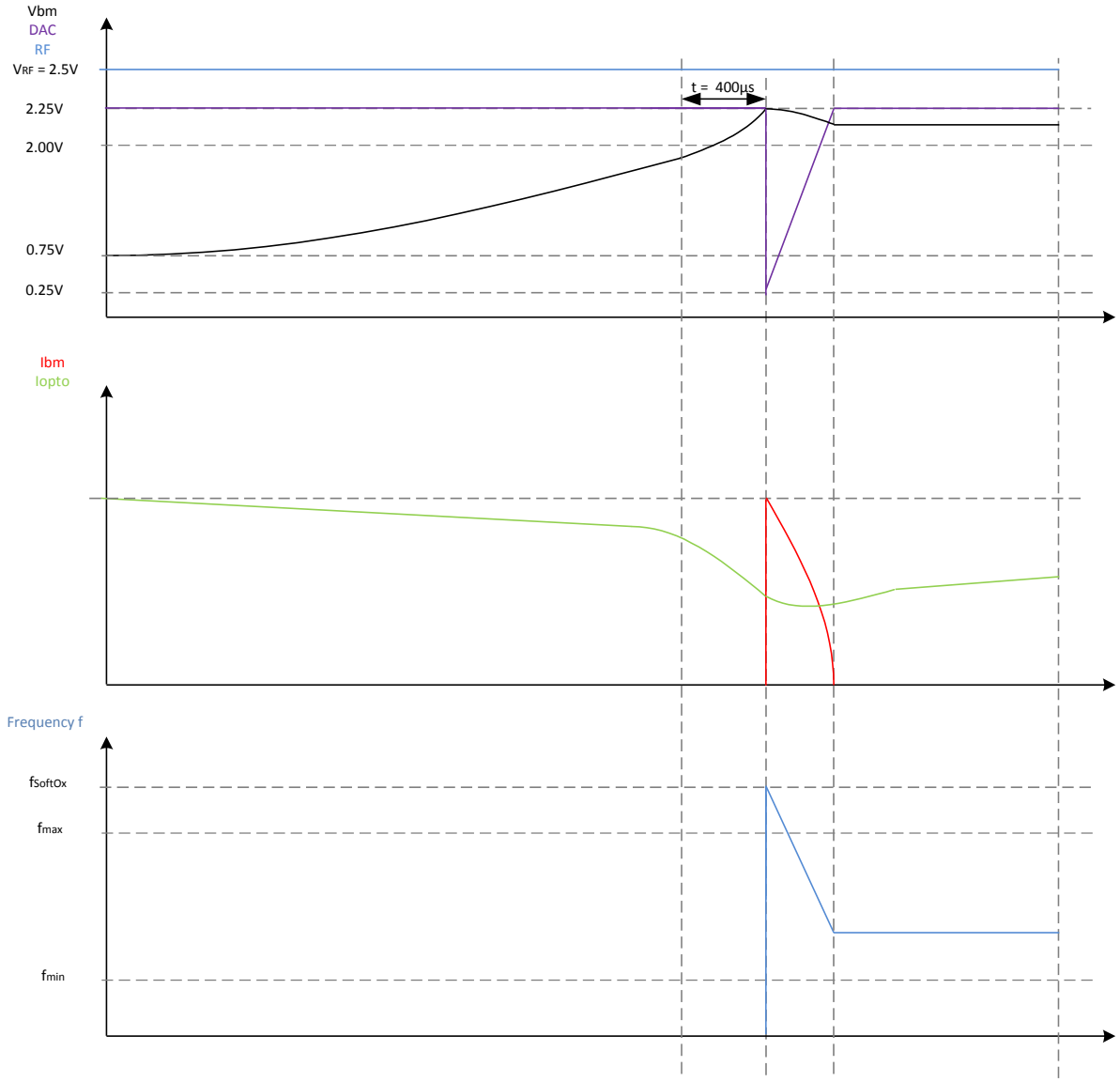

Figure 14: Burst Mode EXIT 1

2.4.2 EXIT 2: Load Step during Burst Pulse (Train)

EXIT 2, in case of a load step during Burst Pulse, the output voltage drops, the internal DAC ramps down and increases the frequency in 7 steps. After the 7 steps, the ICL5102 exits the Burst Mode Operation into normal mode.

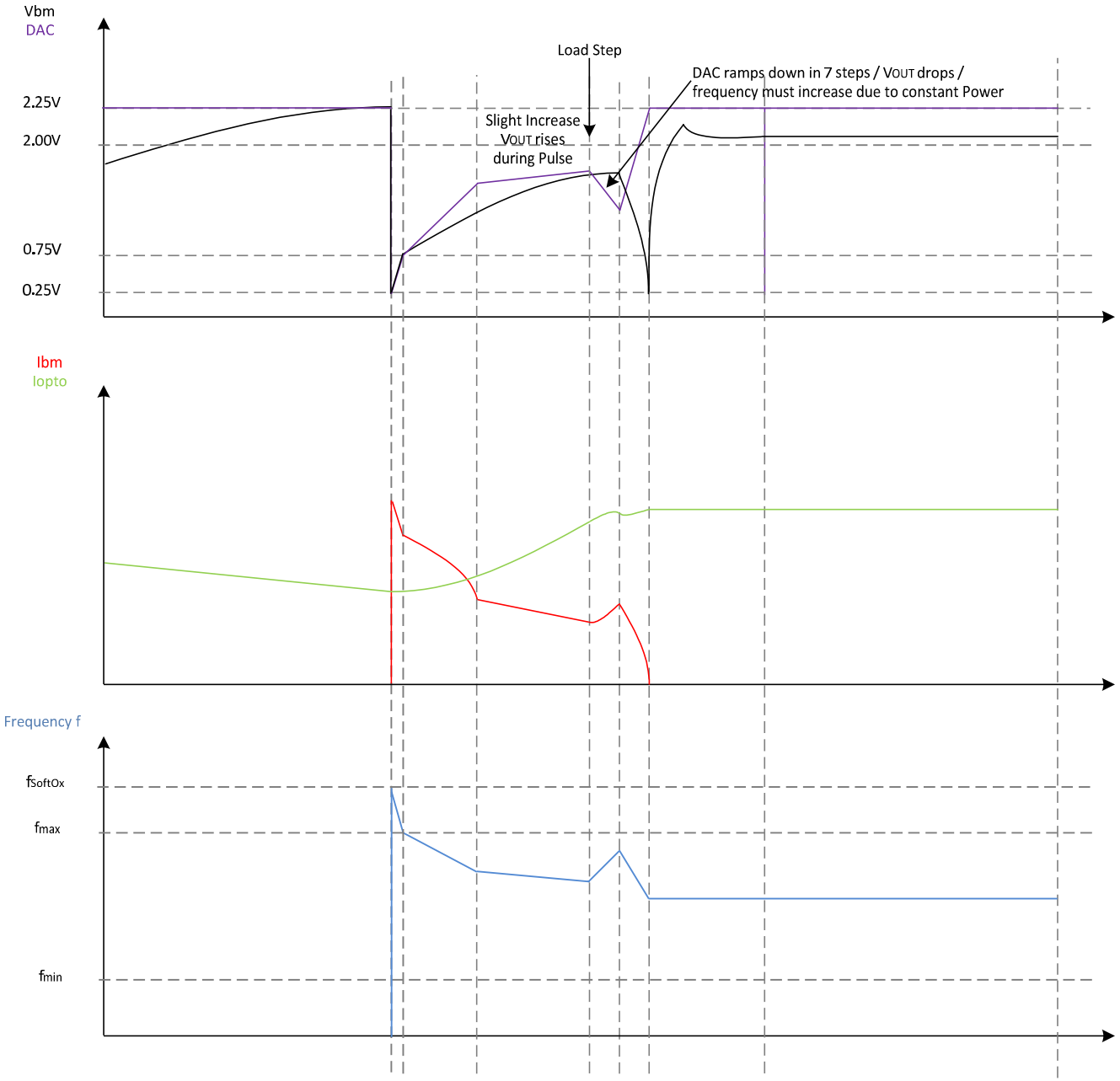

Figure 15: Burst Mode EXIT 2

2.4.3 EXIT 3: Time OUT due to high Static Load

If the Burst Pulse lasts for longer than 10ms, the ICL5102 detects a high static load and exit the Burst Mode Operation.

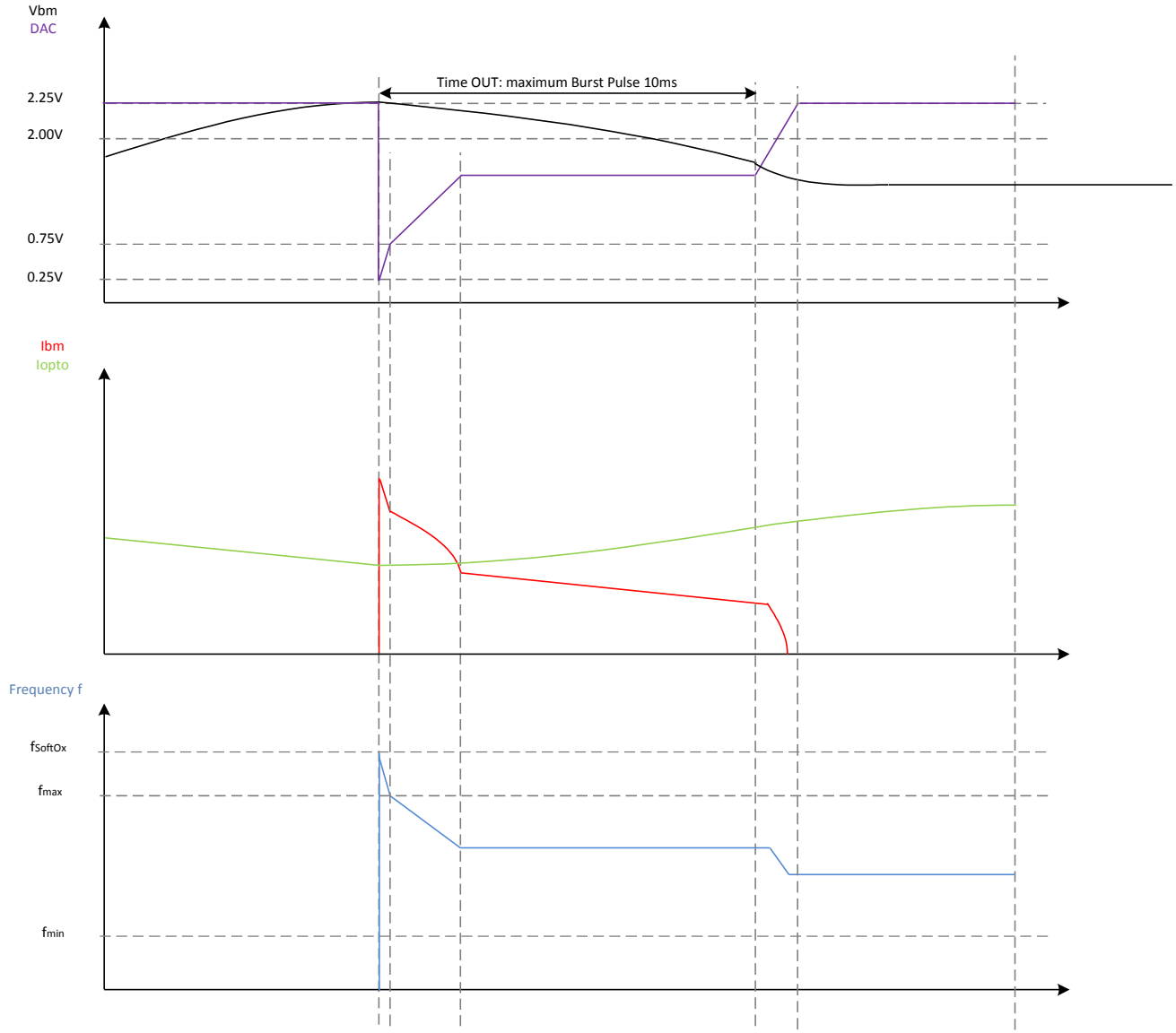

Figure 16: Burst Mode EXIT 3

2.4.4 EXIT 4: Duty Cycle of Burst Pulses due to high Static Load

While high static load, the ICL5102 senses the Burst Pulse and Burst Pause duration. This is a typical EXIT while dimming a LED. An up and down counter with a resolution of 250µs counts in 2 Steps / 250µs during BM Pulse up and while pause 1 step down.

Exit 4 condition:

$t_{BurstPause} < 2 \times t_{BurstPulse}$

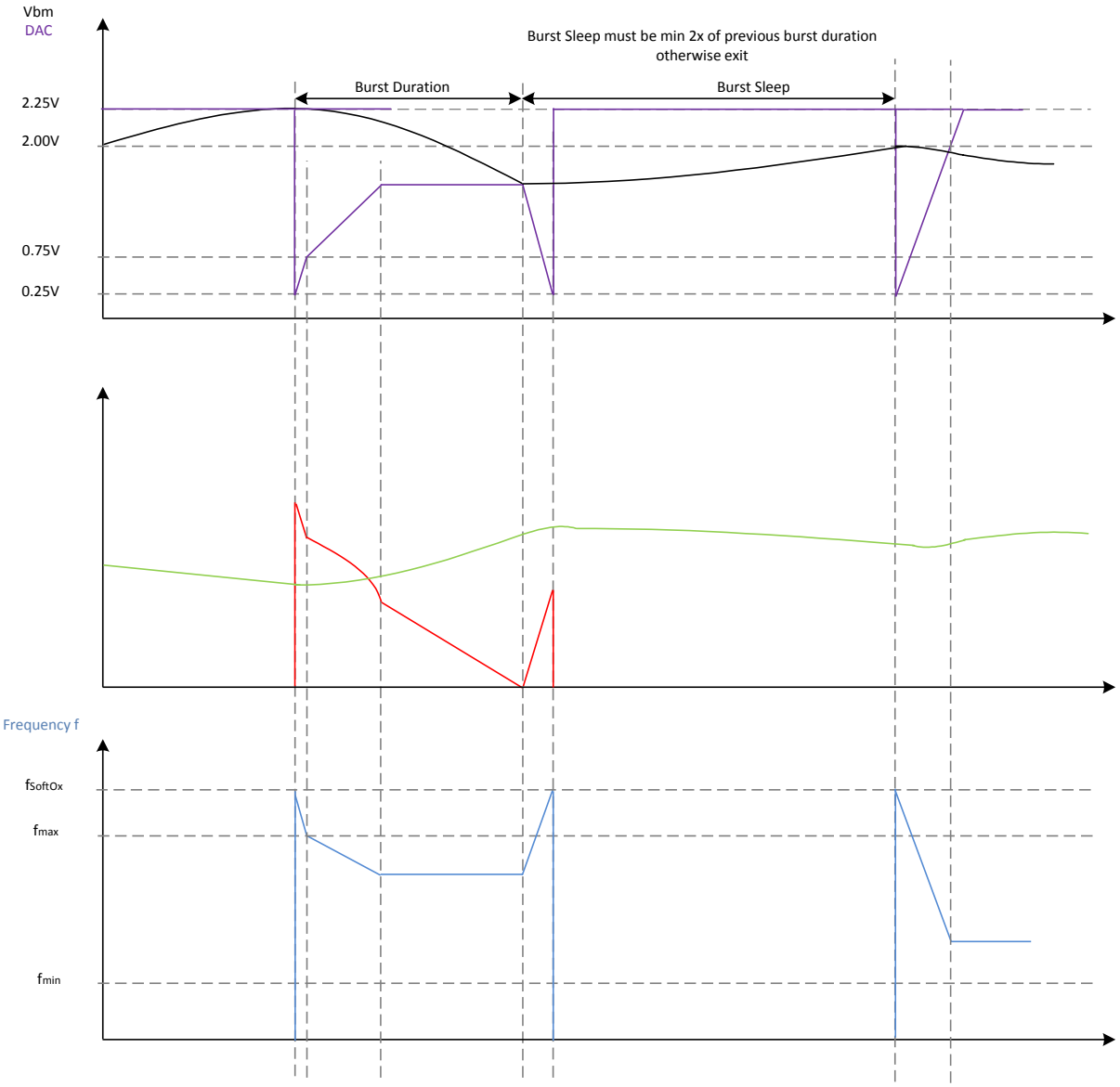

Figure 17: Burst Mode EXIT 4

2.5 Capacitive Load Regulation

The capacitive load regulation is activated if the LSCS threshold will cross V_{LSCS} = +50mV in less than 6% of the period time. The IC increases the frequency in order to leave the area of capacitive mode operation. When the maximum frequency is reached the IC waits for 620µs, powers down and auto restarts.

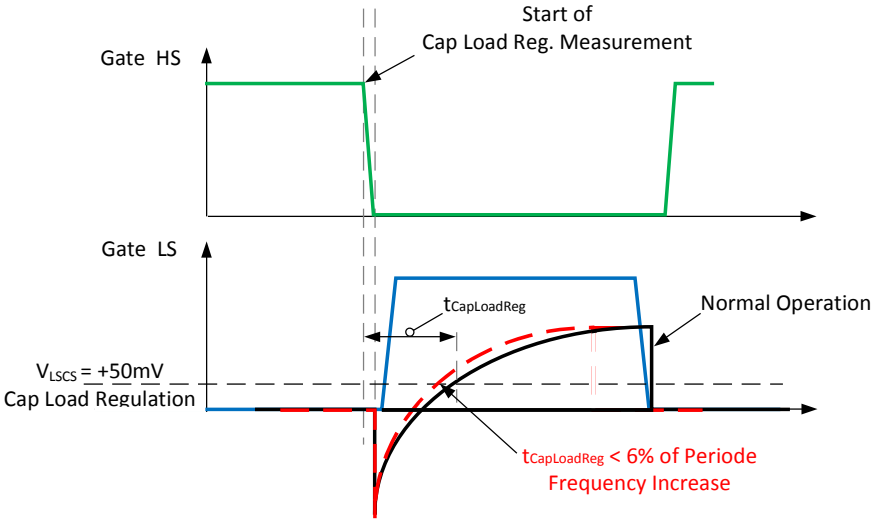

Figure 18: Capacitive Load Regulation

2.6 Self-Adaptive Dead Time

The dead time between the turn OFF and turn ON of the RESONANT drivers is self-adapting and is detected by means of switch-off of the high-side MOSFET and the -50 mV threshold of the LSCS voltage. The typical range of the dead time adjustment is 250 ns up to 750 ns. The start of the dead time measurement is the OFF switching of the high-side MOSFET. The dead time measurement finishes when V_{LSCS} drops below -50 mV for longer than typically 300 ns (internally fixed propagation delay). This time will be stored; the low-side gate driver switches ON. The high-side gate driver turns ON again after OFF switching of the low-side switch and the stored dead time.

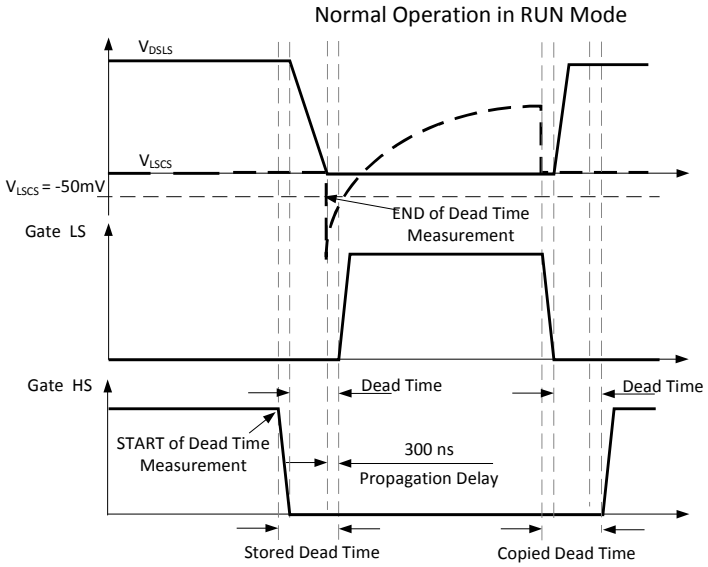

Figure 19: Self-Adaptive Dead Time

3 Bubble Chart

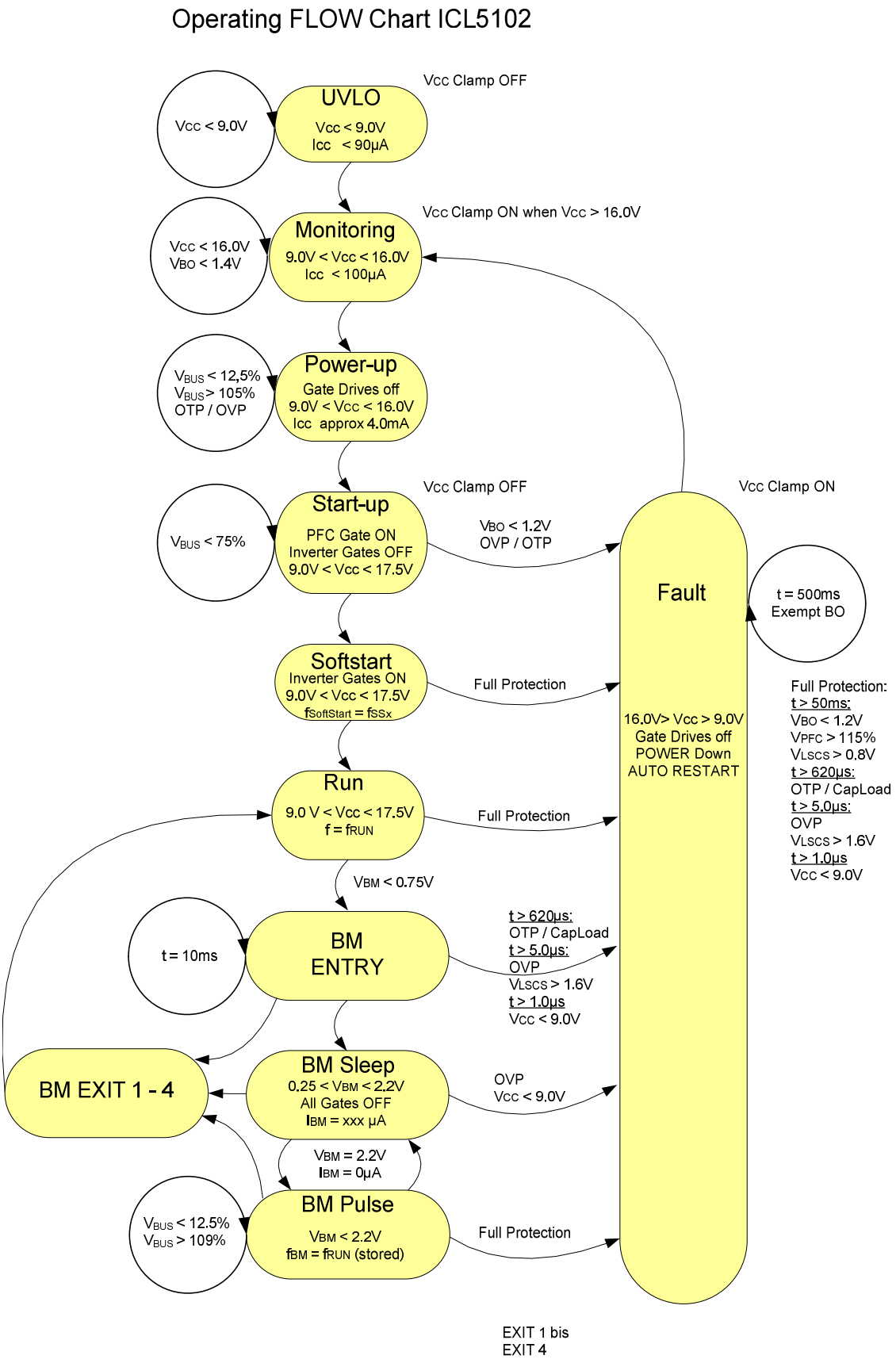

Figure 20: Bubble Chart of internal Processes

4 FAULT Matrix

Description of Fault	Characteristics of Fault			Operating Mode Detection is active							Consequence
	Definition of Fault	Action	Minimum Duration of effect	Monitoring	Power-up 130µs	Start-up	Softstart	Run Mode	Burst PULSE	Burst SLEEP	Reaction
Supply voltage Vcc < 16.0V before power up	Below start-up threshold	W	1µs	X							Prevents Power up
Supply voltage Vcc < 9.0V after power up	Below UVLO threshold	A	1µs	X	X	X	X	X	X	X	Power Down AUTO RESTART
Brown OUT Detection V_{BO} < 1.2V	BO	A	50ms			X	X	X	X		Power Down AUTO RESTART when V_{BO} > 1.4V
Brown IN Control V_{BO} < 1.4V	BI	W	1us	X							Prevents Power up
Over Temperature Detection V_{OTP1} < 703mV	OTP	W	620µs		X						Prevents Power up
Over Temperature Detection V_{OTP2} < 625mV	OTP	A	620µs			X	X	X	X		Power Down AUTO RESTART when V_{OTP} > 703mV
Bus voltage < 12.5% of rated level	Open Loop detection	W	1µs		X						Keep ALL Gate drives off, RESTART when V_{BUS} > 12.5%
Bus voltage < 12.5% of rated level	Open Loop detection	W	1µs			X	X	X	X		Stops PFC FET RESTART when V_{BUS} > 12.5%
Bus voltage < 75% of rated level	PFC Undervoltage	W	1µs			X					Prevents Start Up until V_{BUS} > 75% Keep HB Gate Drives OFF / PFC Gate ON
Bus voltage > 105% of rated level	PFC Overvoltage	W	5µs		X						Keep ALL Gate drives off AUTO RESTARTafter V_{BUS} < 105%
Bus voltage > 109% of rated level	PFC Overvoltage	W	5µs			X	X	X	X		Stops PFC FET RESTART when V_{BUS} < 105%
Bus voltage > 115% of rated level	Inverter Overvoltage	A	50ms				X	X	X		Power Down AUTO RESTART
Output Over Voltage V_{OVP} > 2.5V	OVP	W	5µs		X						Prevents Power up
Output Over Voltage V_{OVP} > 2.5V	OVP	A	5µs			X	X	X	X	X	Stops ALL FETs RESTART when V_{OVP} < 2.5V
Capacitive Load operation below resonance	Cap Load	A	620µs				X	X	X		Power Down AUTO RESTART
Voltage at PFCCS pin V_{PFCCS} > 1.0V	PFC Over Current contr.	N	200ns			X	X	X	X		Stops on-time of PFC FET immediately
Capacitive Load Control	Capacitive Load Control	N	1/2 cycle				X	X			Increase HB frequency
Voltage at LSCS pin V_{LSCS} > 0.8V	Overcurrent Shut down	A	50ms				X	X			Power Down AUTO RESTART
Voltage at LSCS pin V_{LSCS} > 0.8V	overcurrent control	N	1/2 cycle				X	X	X		Increase HB frequency
Voltage at LSCS pin V_{LSCS} > 1.6V	Inverter overcurrent	A	500ns				X	X	X		Power Down AUTO RESTART
N = Normal Condition	W = Wait till Condition										A = Auto-Restart

5 Electrical Characteristics

Note: All voltages except the high-side signals are measured with respect to GND (pin 4). The high-side voltages are measured with respect to pin 14 (HSGND). The voltage levels are valid if other ratings are not violated.

5.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which if exceeded may lead to destruction of the integrated circuit. For the same reason make sure that any capacitor connected to pin 3 (VCC) and pin 15 (HSVCC) is discharged before assembling the application circuit.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
LSCS Voltage	V_{LSCS}	- 5	6	V	
LSCS Current	I_{LSCS}	- 3	3	mA	
LSGD Voltage	V_{LSGD}	- 0.3	V_{cc}+0.3	V	Internally clamped to 11V
LSGD Peak Source Current	$I_{LSGDsomax}$	- 75	5	mA	< 500 ns
LSGD Peak Sink Current	$I_{LSGDsimax}$	- 50	400	mA	< 100 ns
VCC Voltage	V_{VCC}	- 0.3	18.5	V	Use max. 18V Zener Diode
VCC Zener Clamp Current	$I_{VCCzener}$	- 5	5	mA	
PFCGD Voltage	V_{PFCGD}	- 0.3	V_{cc}+0.3	V	Internally clamped to 11V
PFCGD Peak Source Current	$I_{PFCGDsomax}$	- 150	5	mA	< 500 ns
PFCGD Peak Sink Current	$I_{PFCGDsimax}$	- 100	700	mA	< 100 ns
PFCCS Voltage	V_{PFCCS}	- 5	6	V	
PFCCS Current	I_{PFCCS}	- 3	3	mA	
PFCZCD Voltage	V_{PFCZCD}	- 3	6	V	
PFCZCD Current	I_{PFCZCD}	- 5	5	mA	
PFCVS Voltage	V_{PFCVS}	- 0.3	5.3	V	
RFM Voltage	V_{RFM}	- 0.3	5.3	V	
OTP Voltage	V_{OTP}	- 0.3	5.3	V	
OVP Voltage	V_{OVP}	- 0.3	5.3	V	
Burst Mode Voltage	V_{BM}	- 0.3	5.3	V	
Brown Out Voltage	V_{BM}	- 0.3	5.3	V	
HSGND Voltage	V_{HSGND}	- 650	650	V	Referring to GND [1]
HSGND Voltage Transient	dV_{HSGND}/dt	- 40	40	V/ns	
HSVCC Voltage	V_{HSVCC}	- 0.3	18.0	V	Referring to HSGND

[1] Limitation due to creeping distance between the HS & LS Pins (CTT 900V inside)

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
HSGD Voltage	V_{HSGD}	- 0.3	V_{HSVCC}+0.3	V	Internally clamped to 11V
HSGD Peak Source Current	$I_{HSGDsomax}$	- 75	0	mA	< 500ns
HSGD Peak Sink Current	$I_{HSGDsimax}$	0	400	mA	< 100ns
Junction Temperature	T_J	- 40	150	°C	
Storage Temperature	T_S	- 55	150	°C	
Maximum Power Dissipation	P_{TOT}	—	1	W	PG_DSO-16 / T_{amb}=25°C
Thermal Resistance (2 Chips) Junction - Ambient	R_{thJA}	—	125	K/W	PG_DSO-16 @ TA = 85°C & PCB Area > 30x20mm
Soldering Temperature Wave		—	260	°C	Wave Soldering[1)]
Soldering Temperature Reflow		—	[2)]	°C	Reflow Soldering
ESD Capability HBM	V_{ESD_HBM}	—	2	kV	Human Body Model[3)]
ESD Capability CDM	V_{ESD_CDM}	—	1	kV	Charged Device Model[4)]

[1)] According to JESD22A111
[2)] According to J-STD-020D
[3)] According to EIA/JESD22-A114-B
[4)] According to JESD22-C101

5.2 Operating Range

The IC operates as described in the functional description once the values listed here lie within the operating range.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	Max.		
HSVCC Supply Voltage	V_{HSVCC}	$V_{HSVCCOff}$	17.5	V	Referring to HSGND
HSGND Voltage	V_{HSGND}	- 650	650	V	Referring to GND[1)]
VCC Voltage @ 25°C	V_{VCC}	V_{VCCOff}	17.5	V	T_J = 25°C
VCC Voltage @ 125°C	V_{VCC}	V_{VCCOff}	18.0	V	T_J = 125°C
LSCS Voltage Range	V_{LSCS}	- 4	5	V	In active mode
PFCVS Voltage Range	V_{PFCVS}	0	4	V	
PFCCS Voltage Range	V_{PFCCS}	- 4	5	V	In active mode
PFZCD Current Range	I_{PFCZCD}	- 3	3	mA	In active mode
OVP Voltage Range	V_{OVP}	0	2.5	V	
Junction Temperature	T_J	- 40	125	°C	
Adjustable Run Frequency	f_{RF}	20	325	kHz	
Soft Start Frequency max	f_{SSmax}	-	1300	kHz	@ Soft Start
Mains Frequency	f_{Mains}	45	65	Hz	NOTCH Filter Operation

[1)] Limitation due to creeping distance between the HS & LS Pins (CTT 900V inside)

5.3 Characteristics Power Supply Section

Note: The electrical characteristics involve the spread of values given within the specified supply voltage and junction temperature range T_J from -40 °C to 125 °C. Typical values represent the median values, which are given in reference to 25 °C. If not otherwise stated, a supply voltage of 15 V and V_{HSVCC} = 15 V is assumed and the IC operates in active mode. Furthermore, all voltages refer to GND if not otherwise mentioned.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
VCC Quiescent Current	I_{VCCqu1}	—	70	120	µA	V_{VCC} = 8.0V
VCC Supply Current [1]	$I_{VCCSupply}$	—	4.0	5.8	mA	V_{PFCVS} > 2.725V
VCC Supply Current in Auto Restart Mode	$I_{VCCLatch}$	—	100	160	µA	
LSVCC Turn-On Threshold LSVCC Turn-Off Threshold LSVCC Turn-On/Off Hyst.	V_{VCCOn} V_{VCCOff} V_{VCCHys}	15.4 8.5 6.7	16.0 9.0 7.0	16.6 9.5 7.4	V V V	
VCC Zener Clamp Voltage	$V_{VCCClamp}$	15.4	16.3	16.6	V	I_{VCC} = 2mA
VCC Zener Clamp Current	$I_{VCCZener}$	3	—	6	mA	V_{VCC} = 18.0V
High Side Leakage Current	$I_{HSGNDleak}$	—	0.01	2.0	µA	V_{HSGND} = 650V, V_{GND}=0V
HSVCC Quiescent Current	$I_{HSVCCqu1}$ [2]	—	190	280	µA	V_{HSVCC} = 8.0V
HSVCC Supply Current[1]	$I_{HSVCCqu2}$ [2]	—	0.65	1.2	mA	V_{HSVCC} > $V_{HSVCCOn}$
HSVCC Turn-On Threshold HSVCC Turn-Off Threshold HSVCC Turn-On/Off Hyst.	$V_{HSVCCOn}$ [2] $V_{HSVCCOff}$ [2] $V_{HSVCCHy}$ [2]	9.55 7.9 1.4	10.3 8.6 1.7	11.0 9.3 2.1	V V V	
Low Side Ground	GND					

[1] With inactive gate
[2] Refers to high-side ground (HSGND)

5.4 Characteristics of PFC Section

5.4.1 PFC Current Sense (PFCCS)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Turn-off threshold	$V_{PFCCSOff}$	0.95	1.0	1.05	V	
Overcurrent blanking + propagation delay[1)]	$t_{PFCCSOff}$	140	200	260	ns	
Leading-edge blanking	$t_{Blanking}$	180	250	315	ns	Pulse width when V_{PFCCS} > 1.0V
PFCCS bias current	$I_{PFCCSBias}$	- 0.5	—	0.5	µA	V_{PFCCS} = 1.5V

[1)] Propagation Delay = 50 ns

5.4.2 PFC Zero Current Detection (PFCZCD)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Zero crossing upper thr. [1)]	$V_{PFCZCDUp}$	1.4	1.5	1.6	V	
Zero crossing lower thr. [2)]	$V_{PFCZCDLow}$	0.4	0.5	0.6	V	
Zero crossing hysteresis	$V_{PFCZCDHys}$	—	1.0	—	V	
Clamping of pos. voltages	$V_{PFCZCDpclp}$	4.1	4.6	5.10	V	$I_{PFCZCDSink}$ = 2mA
Clamping of neg. voltages	$V_{PFCZCDnclp}$	- 1.70	- 1.4	- 1.0	V	$I_{PFCZCDSource}$ = - 2mA
PFCZCD bias current	$I_{PFCZCDBias}$	- 0.5	—	5.0	µA	V_{PFCZCD} = 1.5V
PFCZCD bias current	$I_{PFCZCDBias}$	- 0.5	—	0.5	µA	V_{PFCZCD} = 0.5V
PFCZCD ringing su.[3)] time	$t_{Ringsup}$	350	500	650	ns	
Limit value for ON time extension	$_{\Delta}t \times I_{ZCD}$	400	600	670	pC	

[1)] Turn-OFF threshold
[2)] Turn-ON threshold
[3)] Ringing suppression time

5.4.3 PFC Voltage Sensing Bus (PFCVS)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	Typ.	max.		
Trimmed reference voltage	$V_{PFCVSRef}$	2.46	2.50	2.54	V	
Overvoltage turn-off (115 %)	$V_{PFCVSUp1}$	2.82	2.88	2.93	V	
Overvoltage turn-off (109 %)	$V_{PFCVSUp2}$	2.67	2.73	2.78	V	
Overvoltage turn-on (105 %)	$V_{PFCVSLow}$	2.56	2.63	2.68	V	
Overvoltage hysteresis	$V_{PFCVSHys}$	70	100	130	mV	4 % rated bus voltage
Rated bus voltage (95 %)	$V_{PFCVS95}$	2.32	2.38	2.425	V	
Undervoltage (75 %)	$V_{PFCVSUV1}$	1.83	1.88	1.92	V	
Undervoltage (12.5 %)	$V_{PFCVSUV2}$	0.237	0.31	0.387	V	
PFCVS bias current	$I_{PFCVSBias}$	- 1.0	—	1.0	µA	V_{PFCVS} = 2.5V

5.4.4 PFC PWM Generation

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	Typ.	max.		
Initial ON time [1]	$t_{PFCON\_initial}$	1.75	6.0	10.64	µs	V_{PFCZCD} = 0V, V_{BO} = 2.0V
Max. ON time [2]	t_{PFCON_max}	17	22.0	26	µs	@ V_{ACIN} = 90V
Switch threshold from CrCM to DCM	t_{PFCON_min}	100	220	370	ns	
Repetition time [1]	t_{PFCRep}	47	52	60	µs	V_{PFCZCD} = 0V
Off time	t_{PFCOff}	42	47	52.5	µs	

[1] When missing zero crossing signal
[2] At the maximum of the AC line input voltage in RUN Mode

5.4.5 PFC Gate Drive (PFCGD)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	Typ.	max.		
PFCGD Low Voltage	$V_{PFCGDLow}$	0.40	0.70	0.92	V	I_{PFCGD} = 5mA
		0.40	0.75	1.12	V	I_{PFCGD} = 20mA
		- 0.20	0.30	0.62	V	I_{PFCGD} = -20mA
PFCGD High Voltage	$V_{PFCGDHigh}$	10.0	11.0	11.6	V	I_{PFCGD} = -20mA
		7.5	—	—	V	I_{PFCGD} = -1mA / V_{VCC} [1]
		7.0	—	—	V	I_{PFCGD} = -5mA / V_{VCC} [1]
PFCGD active Shut Down	$V_{PFCGASD}$	0.40	0.75	1.12	V	I_{PFCGD} = 20mA V_{VCC}=5V
PFCGD UVLO Shut Down	$V_{PFCGDuvlo}$	0.30	1.00	1.60	V	I_{PFCGD} = 5mA V_{VCC}=2V
PFCGD Peak Source Current	$I_{PFCGDSource}$	—	- 100	—	mA	[2] + [3]
PFCGD Peak Sink Current	$I_{PFCGDSink}$	—	500	—	mA	[2] + [3]
PFCGD Voltage during sink Current	$V_{PFCGDHigh}$	10.8	11.7	12.3	V	$I_{PFCGDSinkH}$ = 3mA
PFC Rise Time	$t_{PFCGDRise}$	70	245	570	ns	2V > VLSGD < 8V [2]
PFC Fall Time	$t_{PFCGDFall}$	20	45	72	ns	8V > VLSGD > 2V [2]

[1] V_{VCC} = V_{VCCOff} + 0.3V
[2] R_{Load} = 4Ω and C_{Load} = 3.3nF
[3] The parameter is not subject to production testing – verified by design/characterization

5.5 Characteristics of Inverter Section

5.5.1 Low-Side Current Sense (LSCS)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Overcurrent shutdown volt. 1	$V_{LSCSOvC1}$	1.54	1.6	1.66	V	
Duration of overcurrent 1	$t_{LSCSOvC1}$	430	600	670	ns	
Overcurrent shutdown Volt. 2	$V_{LSCSOvC2}$	0.74	0.8	0.86	V	
Duration of overcurrent 2	$t_{LSCSOvC2}$	—	50	—	ms	1)
Capacitive mode det. Level 1	$V_{LSCSCap1}$	1.54	1.6	1.66	V	during turn-ON of the HSGD
Capacitive mode duration 1	$t_{LSCSCap1}$	30	50	90	ns	
Capacitive mode det. Level 2	$V_{LSCSCap2}$	- 70	- 50	- 25	mV	before turn-ON of the HSGD
Capacitive mode duration 2	$t_{LSCSCap2}$	280	280	520	ns	
Capacitive load control regulation voltage	$V_{LSCSCapC}$	25	50	70	mV	
Capacitive load control regulation ratio	$R_{LSCSCapC}$	4.5	7	9	%	
Over Current Control	V_{LSCSCC}	0.74	0.8	0.86	V	
LSCS bias current	$I_{LSCSBias}$	-1.0	—	1.0	µA	@ V_{LSCS} = 1.5 V

1) The parameter is not subject to production testing – verified by design/characterization

5.5.2 Low-Side Gate Drive (LSGD)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
LSGD low voltage	$V_{LSGDLow}$	0.40	0.70	1.00	V	I_{LSGD} = 5 mA
		0.40	0.80	1.20	V	I_{LSGD} = 20 mA
		- 0.30	0.20	0.53	V	I_{LSGD} = - 20 mA
LSGD high voltage	$V_{LSGDHigh}$	10.0	10.8	11.6	V	I_{LSGD} = - 20 mA
		7.5	—	—	V	I_{LSGD} = –1 mA 1)
		7.0	—	—	V	I_{LSGD} = –5 mA 1)
LSGD active shutdown	$V_{LSGDASD}$	0.4	0.75	1.12	V	I_{LSGD} = 20 mA / V_{CC} = 5V
LSGD UVLO shutdown	$V_{LSGDUVLO}$	0.3	1.0	1.6	V	I_{LSGD} = 5 mA / V_{CC} = 2 V
LSGD peak source current	$I_{LSGDSource}$	—	- 50	—	mA	2) + 3)
LSGD peak sink current	$I_{LSGDSink}$	—	300	—	mA	2) + 3)
LSGD voltage during sink Current	$V_{LSGDHigh}$	—	11.7	—	V	$I_{LSGDsinkH}$ = 3 mA
LSGD rise time	$t_{LSGDRise}$	70	245	570	ns	2 V < V_{LSGD} < 8 V 2)
LSGD fall time	$t_{LSGDFall}$	20	35	60	ns	8 V > V_{LSGD} > 2 V 2)

1) $V_{CC} = V_{CCOFF}$ + 0.3 V
2) Load: R_{Load} = 10 Ω and C_{Load} = 1 nF
3) The parameter is not subject to production testing – verified by design/characterization

5.5.3 Inverter Run Frequency (RF)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
RF voltage in run mode	V_{RF}	2.46	2.5	2.54	V	@ 100µA<I_{RFM}<800µA
	I_{RFmax}	-1.6		-0.6	mA	
Run frequency	f_{RF}	92.5	95	97.5	kHz	R_{RF} = 10kΩ
Adjustable run frequency	f_{RF1}	36	38	41	kHz	I_{RF} = - 100 µA
	f_{RF2}	73	76	79	kHz	I_{RF} = - 200 µA
	f_{RF3}	114	185	200	kHz	I_{RF} = - 500 µA
	f_{RF4}	140	220	240	kHz	I_{RF} = - 600 µA[1)]
	f_{RF5}	190	290	325	kHz	I_{RF} = - 800 µA[1)]

[1)] Run frequency T_J > - 25°C

5.5.4 Burst Mode Operation (BM)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Burst Mode Thresholds	$V_{BMEntry}$	710	750	790	mV	
	$t_{BMEntry}$	8.5	10.0	11.5	ms	
	$V_{BMStart}$	2.13	2.20	2.27	V	
	V_{BMExit}	1.93	2.0	2.07	V	
	I_{BMmax}		800		µA	
	I_{BMStop}	-3	—	14	µA	

5.5.5 Brownout Detection (BO)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Brownout Detection ON	V_{BOON}	1.14	1.2	1.26	V	
Brownout Detection Leave	$V_{BOLeave}$	1.34	1.4	1.46	V	
BO Bias Current	I_{BOBias}	-0.5	—	0.5	µA	V_{BO} = 5.0V

5.5.6 Overvoltage Protection (OVP)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
OVP Reference Voltage	V_{OVP_Ref}	2.45	2.5	2.55	V	t > 5µs
OVP Bias Current	I_{OVP_Bias}	- 0.5	—	0.5	µA	V_{OVP} = 3.0V

5.5.7 Over Temperature Protection (OTP) for NTC

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Over Temperature Protection	V_{OTP1}	670	703	735	mV	
	V_{OTP2}	594	625	665	mV	
Over Temperature Protection Current	I_{OTP}	- 106	- 100	- 94	µA	

5.5.8 High Side Gate Drive (HSGD)

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	typ.	max.		
HSGD Low Voltage	$V_{HSGDLow}$	0.018	0.05	0.1	V	I_{HSGD} = 5mA
		0.40	1.10	2.50	V	I_{HSGD} = 100mA
		- 0.40	-0.20	- 0.04	V	I_{LSGD} = - 20mA
HSGD High Voltage	$V_{HSGDHigh}$	9.7	10.5	11.3	V	V_{CCHS}=15V I_{HSGD} = - 20mA
		7.8	—	—	V	$V_{CCHSOFF}$ + 0.3V I_{HSGD} = - 1mA
HSGD active Shut Down	$V_{HSGDASD}$	0.04	0.22	0.50	V	V_{CCHS}=5V I_{HSGD} = 20mA
HSGD Peak Source Current	$I_{HSGDSource}$	—	- 50	—	mA	R_{Load} = 10Ω+C_{Load} = 1nF [1)]
HSGD Peak Sink Current	$I_{HSGDSink}$	—	300	—	mA	R_{Load} = 10Ω+C_{Load} = 1nF [1)]
HSGD Rise Time	$t_{HSGDRise}$	120	220	320	ns	2V < V_{LSGD} < 8V R_{Load} = 10Ω+C_{Load} = 1nF
HSGD Fall Time	$t_{HSGDFall}$	17	35	70	ns	8V > V_{LSGD} > 2V R_{Load} = 10Ω+C_{Load} = 1nF

[1)] The parameter is not subject to Production Test – verified by Design / Characterization

5.6 Timing Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	typ.	max.		
Inverter Dead Time max_1	$t_{Deadmax1}$	550	750	930	ns	LSCS > - 50mV / 100kHz
Inverter Dead Time max_2	$t_{Deadmax2}$	350	500	600	ns	LSCS > - 50mV / 325kHz
Inverter Dead Time min	$t_{Deadmin}$	150	250	300	ns	LSCS < - 50mV / 325kHz

6 Outline Dimension

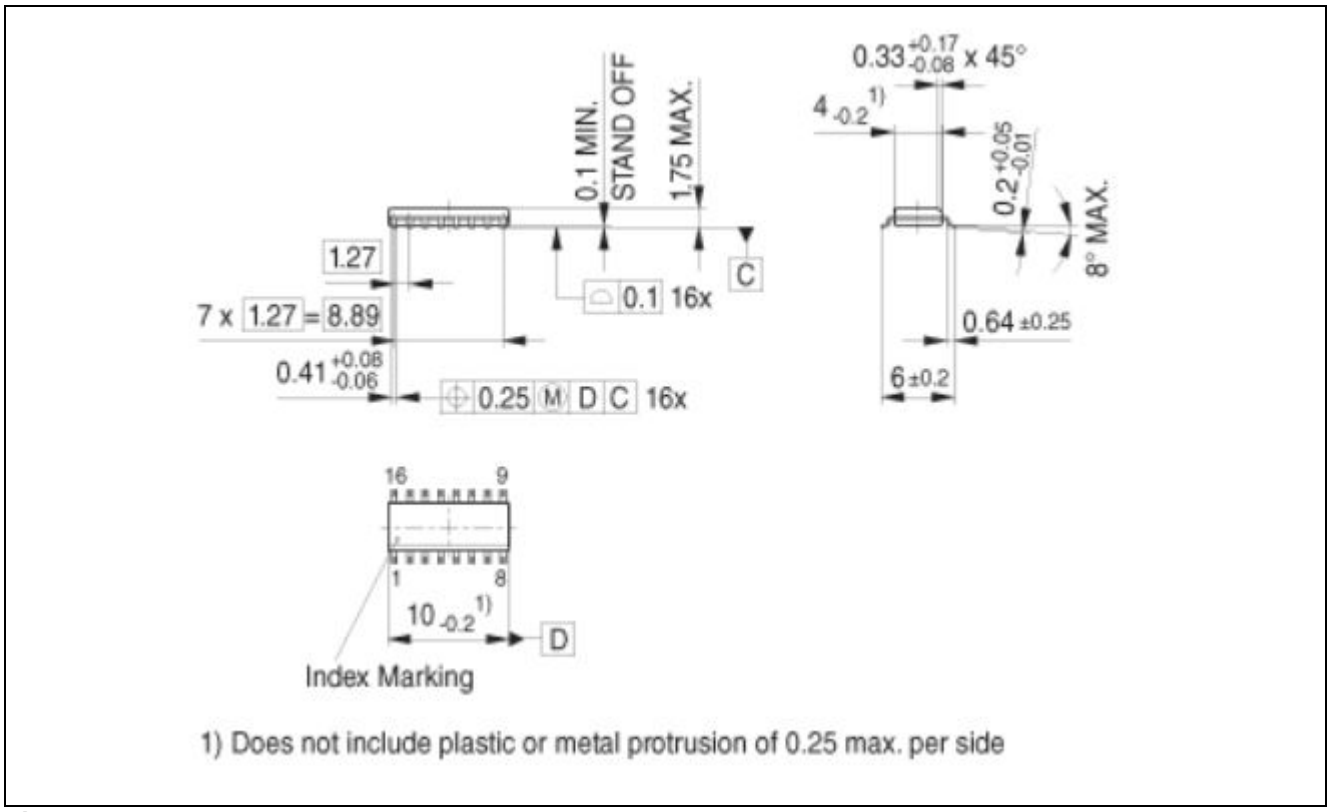

Figure 21 PG-DSO-16

Notes

1. *You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": **http://www.infineon.com/products**.*
2. *Dimensions in mm.*

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