LED Controller IC

Single Stage PFC and Flyback LED Controller

ICL8002G

Data Sheet

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1 Single Stage PFC and Flyback LED Controller Product Highlights

- Primary side control significantly reduces BOM enabling lowest system cost,smallest form factor and simplified design.
- Advance quasi-resonant opreation for leading and traling edge dimmers
- High efficiency over wide dimming range.
- Continuous dimming curve and stabilized light output.
- Enabling high PF upto 98% and low THD <10%.

Features

- HV startup cell for short time to light and high driver efficiency.
- Digital foldback correction for good line regulation capability.
- Precise PWM for primary PFC and dimming control.
- Support various protection modes.
- Digital soft-start.
- VCC over/ under-voltage protection.
- Auto restart mode for short circuit protection
- Cycle-by-cycle peak current limitation.

Description

The ICL8002G is designed for the offline LED lighting applications with high efficiency requirements.It provides a single stage Flyback and buck solution with high power factor correction(PFC) and dimming functionality. Innovative primary side control techniques combined with accurate PWM generation for phase cut dimming which enables LED lamp/luminaire with significantly reduced component count for smallest form factor and simplified design.

ICL8002G employs quasi-resonant operation mode optmized for leading and trailing edge phase-cut dimmers used LED lamps,tubes or down lights.Dimming performance can be improved even further by external bleeder and damper circuitry. Primary side control enables high power factor >98% and low THD<10%, improving the driver efficiency significantly upto 90%. The ICL8002G has multiple safety functions that ensure a full system protection.

ICL8002G represents an outstanding choice for quasi-resonant Flyback and buck LED lamp designs combining a taliored feature set and performance at minimum BOM cost.

Application Circuit for Primary Control

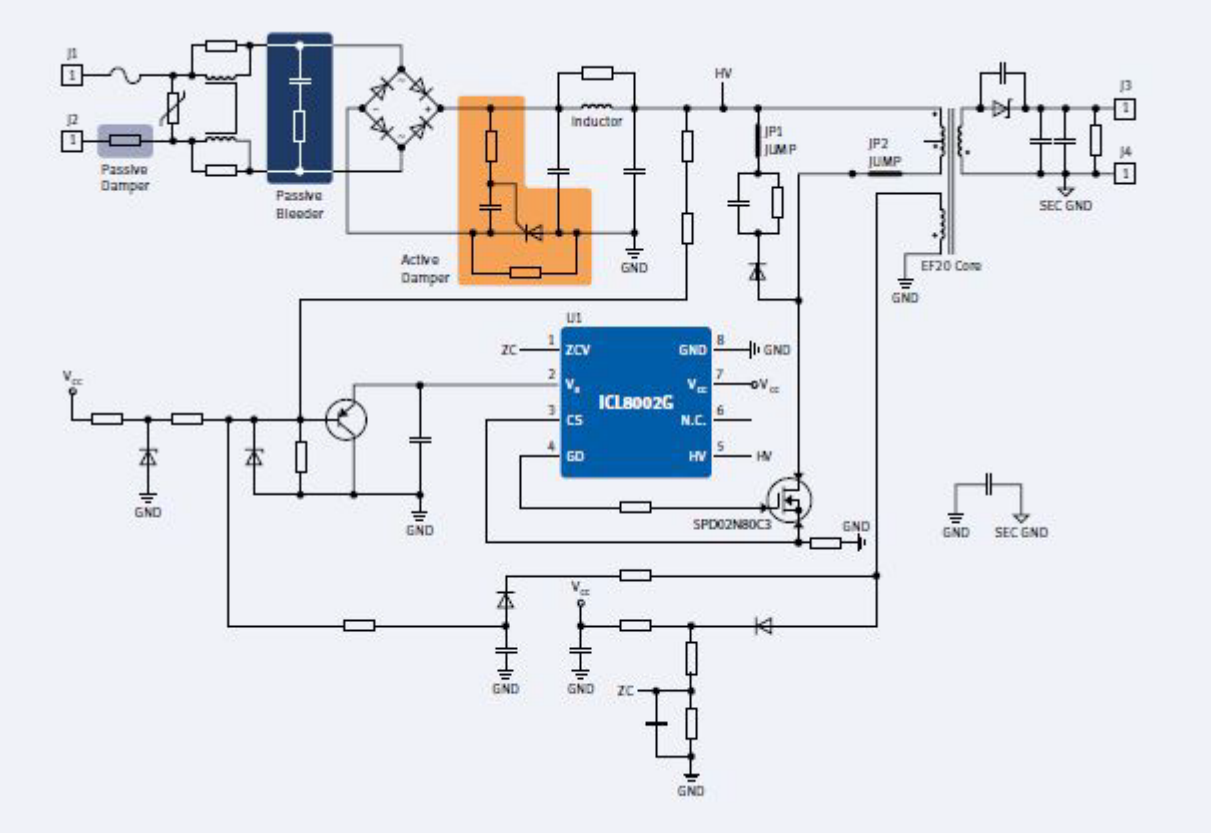


Figure 1 Application Circuit

Type	Package
ICL8002G	PG-DSO-8

2 Pin Configuration and Functionality

2.1 Pin Configuration with PG-DSO-8

Table 1 Pin Description

Ball No.	Name	Pin Type	Buffer Type	Function
1	ZCV	–	–	**Zero Crossing**
2	VR	–	–	**Voltage Sense**
3	CS	–	–	**Current Sense**
4	GD	–	–	**Gate Drive Output**
5	HV	–	–	**High Voltage Input**
6	n.c.	–	–	**Not connected**
7	VCC	–	–	**Controller Supply Voltage**
8	GND	GND	–	**Controller Ground**

2.2 Package PG-DSO-8

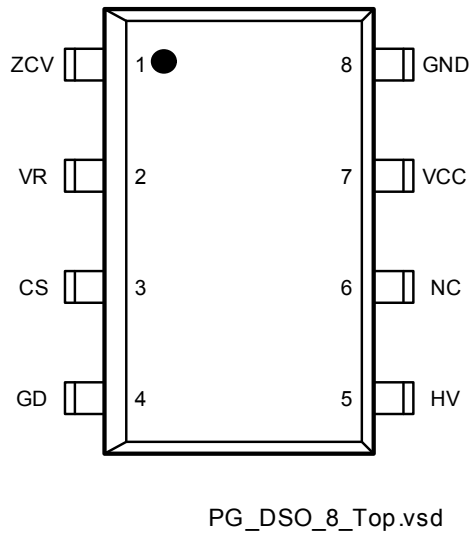


Figure 2 Pin Configuration PG-DSO-8(top view)

2.3 Pin Functionality

ZCV (Zero Crossing)

At this pin, the voltage from the auxiliary winding after a time delay circuit is applied. Internally, this pin is connected to the zero-crossing detector for switch-on determination. Additionally, the output overvoltage detection is realized by comparing the voltage Vzc with an internal preset threshold.

VR (Voltage Sense)

The rectified input mains voltage is sensed at this pin. The signal is used to set the peak current of the peak-current control and therefore allow for the PFC and phase-cut dimming functionality.

CS (Current Sense)

This pin is connected to the shunt resistor for the primary current sensing, externally, and the PWM signal generator for switch-off determination (together with the feedback voltage), internally. Moreover, short-winding protection is realised by monitoring the voltage Vcs during on-time of the main power switch.

GD (Gate Drive Output)

This output signal drives the external main power switch, which is a power MOSFET in most case.

HV (High Voltage)

The pin HV is connected to the bus voltage, externally, and to the power cell, internally. The current through this pin pre-charges the VCC capacitor with constant current once the supply bus voltage is applied.

VCC (Power supply)

VCC pin is the positive supply of the IC. The operating range is between V_{VCCoff} and V_{VCCOVP}.

GND (Ground)

This is the common ground of the controller.

3 Representative Block Diagram

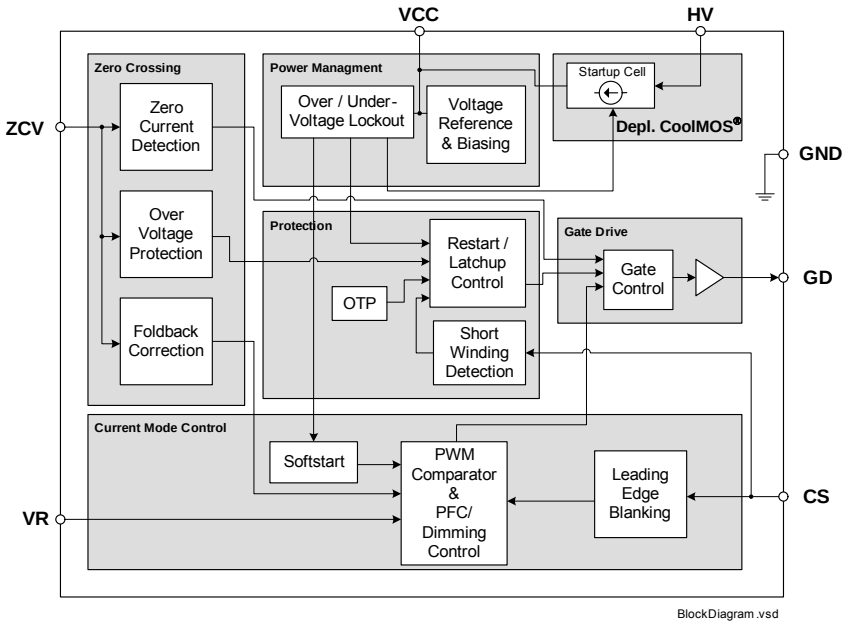


Figure 3 Representative Block Diagram

4 Functional Description

4.1 VCC Pre-Charging and Typical VCC Voltage During Start-up

In ICL8002G, a high voltage startup cell is integrated. As shown in Figure 2, the start cell consists of a high voltage device and a controller, whereby the high voltage device is controlled by the controller. The startup cell provides a pre-charging of the VCC capacitor till VCC voltage reaches the VCC turned-on threshold V_{VCCon} and the IC begins to operate.

Once the mains input voltage is applied, a rectified voltage shows across the capacitor Cbus. The high voltage device provides a current to charge the VCC capacitor C_{VCC}. Before the VCC voltage reaches a certain value, the amplitude of the current through the high voltage device is only determined by its channel resistance and can be as high as several mA. After the VCC voltage is high enough, the controller controls the high voltage device so that a constant current around 1mA is provided to charge the VCC capacitor further, until the VCC voltage exceeds the turned-on threshold V_{VCCon}. As shown as the time phase I in Figure 3, the VCC voltage increase near linearly and the charging speed is independent of the mains voltage level.

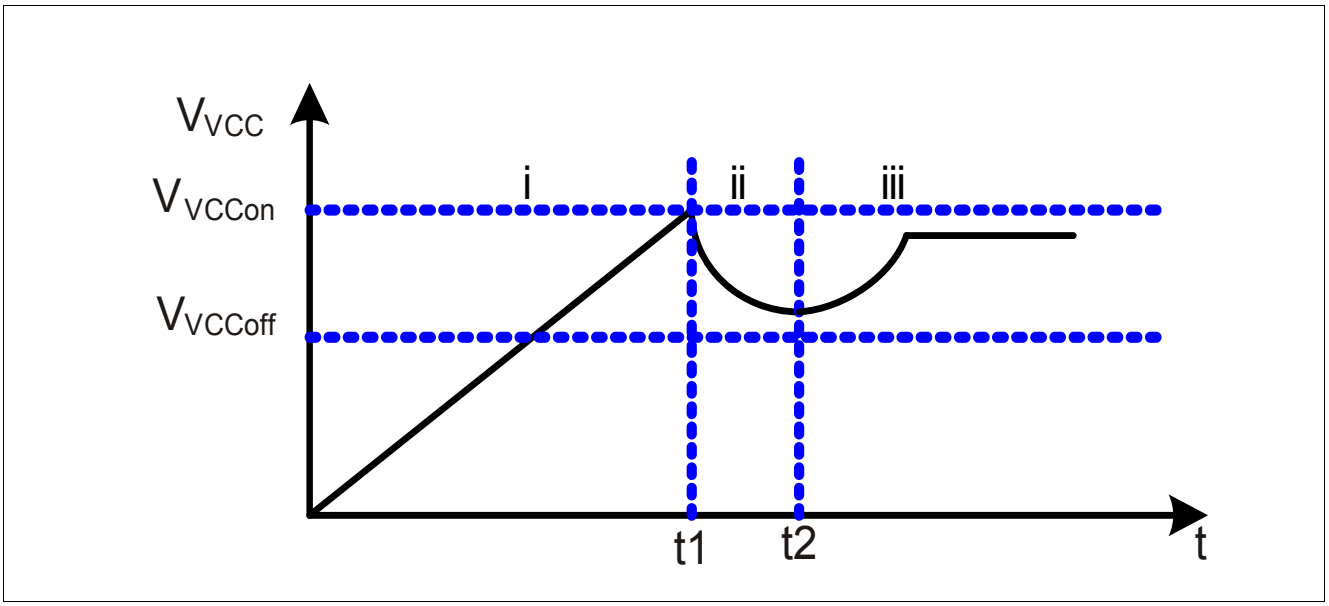


Figure 4 VCC voltage at start up

The time taking for the VCC pre-charging can then be approximately calculated as:

$$t_1 = \frac{V_{VCCon} \cdot C_{VCC}}{I_{VCCcharge2}} \quad (1)$$

where IVCCcharge2 is the charging current from the startup cell which is 1.05mA, typically.

Exceeds the VCC voltage the turned-on threshold V_{VCCon} of at time t1, the startup cell is switched off, and the IC begins to operate with a soft-start. Due to power consumption of the IC and the fact that still no energy from the auxiliary winding to charge the VCC capacitor before the output voltage is built up, the VCC voltage drops (Phase II). Once the output voltage is high enough, the VCC capacitor receives then energy from the auxiliary winding from the time point t2 on. The VCC then will reach a constant value depending on output load.

4.2 Soft-start

At the time ton, the IC begins to operate with a soft-start. By this soft-start the switching stresses for the switch, diode and transformer are minimised. The soft-start implemented in ICL8002G is a digital time-based function. The preset soft-start time is 12ms with 4 steps. If not limited by other functions, the peak voltage on CS pin will increase step by step from 0.32 V to 1 V finally.

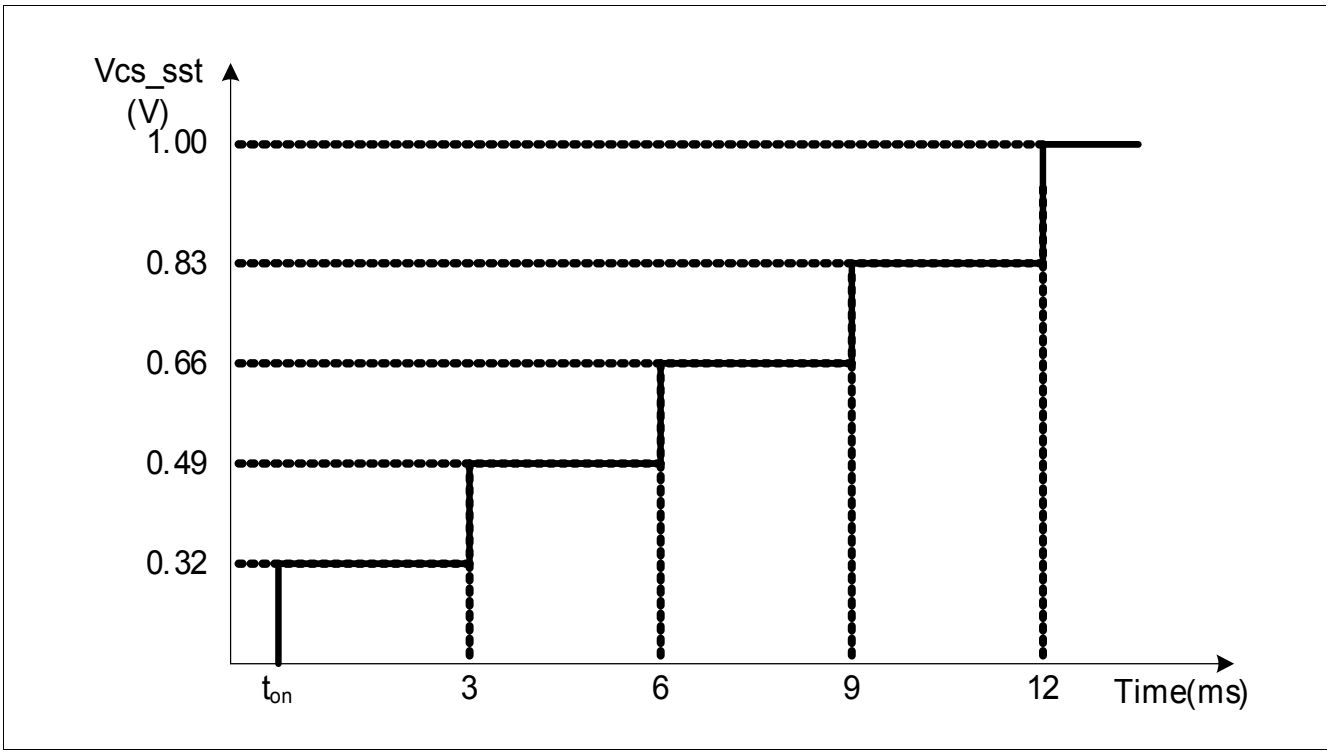


Figure 5 Maximum current sense voltage during softstart

4.3 Normal Operation

The PWM controller during normal operation consists of a digital signal processing circuit including a comparator, and an analog circuit including a current measurement unit and a comparator. The switch-on and -off time points are each determined by the digital circuit and the analog circuit, respectively. As input information for the switch-on determination, the zero-crossing input signal is needed, while the voltages sense signal at pin VR and the current sensing signal V_{CS} are necessary for the switch-off determination. Details about the full operation of the PWM controller in normal operation are illustrated in the following paragraphs.

4.3.1 Zero Crossing

In the system, the voltage from the auxiliary winding is applied to the zero-crossing pin through a RC network, which provides a time delay to the voltage from the auxiliary winding. Internally, this pin is connected to a clamping network, a zero-crossing detector, an output overvoltage detector and a ringing suppression time controller.

During on-state of the power switch a negative voltage applies to the ZCV pin. Through the internal clamping network, the voltage at the pin is clamped to -0.3V.

The voltage V_{ZC} is also used for the output overvoltage protection. Once the voltage at this pin is higher than the threshold V_{ZCOVP} during off-time of the main switch, the IC is latched off after a fixed blanking time.

To achieve the switch-on at voltage valley, the voltage from the auxiliary winding is fed to a time delay network (the RC network consists of Dzc, Rzc1, Rzc2 and Czc as shown in typical application circuit) before it is applied to the zero-crossing detector through the ZC pin. The needed time delay to the main oscillation signal Dt should be approximately one fourth of the oscillation period (by transformer primary inductor and drain-source capacitor)

minus the propagation delay from thedetected zero-crossing to the switch-on of the main switch tdelay, theoretically:

$$\Delta t = \frac{T_{OSC}}{4} - t_{delay} \tag{2}$$

This time delay should be matched by adjusting the time constant of the RC network which is calculated as:

$$\tau_{td} = C_{ZC} \cdot \frac{R_{ZC\,1} \cdot R_{ZC\,2}}{R_{ZC\,1} + R_{ZC\,2}} \tag{3}$$

4.3.2 Ringing Suppression Time

After MOSFET is turned off, there will be some oscillation on VDS, which will also appear on the voltage on ZC pin. To avoid that the MOSFET is turned on mistriggerred by such oscillations, a ringing suppression timer is implemented. The timer is dependent on the voltage V_{ZC}. When the voltage V_{ZC} is lower than the threshold V_{ZCRS}, a longer preset time applies, while a shorter time is set when the voltage V_{ZC} is higher than the threshold.

4.3.2.1 Switch on Determination

After the gate drive goes to low, it can not be changed to high during ring suppression time.

After ring suppression time, the gate drive can be turned on when the zero crossing is detected.

However, it is also possible that the oscillation between primary inductor and drain-source capacitor damps very fast and IC can not detect a zero crossing. In this case, a maximum off time is implemented. After gate drive has been remained off for the period of t_{OffMax}, the gate drive will be turned on again regardless. This function can effectively prevent the switching frequency from going lower than 20kHz, otherwise which will cause audible noise, during start up.

4.3.3 Switch Off Determination

In the converter system, the primary current is sensed by an external shunt resistor, which is connected between low-side terminal of the main power switch and the common ground. The sensed voltage across the shunt resistor V_{CS} is applied to an internal current measurement unit, and its output voltage V1 is compared with the voltage at pin VR. Once the voltage V1 exceeds the voltage V_{VR}, the output flip-flop is reset. As a result, the main power switch is switched off. The relationship between the V1 and the V_{CS} is described by:

$$V_1 = 3.3 \cdot V_{CS} + 0.7 \tag{4}$$

To avoid mistriggering caused by the voltage spike across the shunt resistor at the turn on of the main power switch, a leading edge blanking time, t_{LEB}, is applied to the output of the comparator. In other words, once the gate drive is turned on, the minimum on time of the gate drive is the leading edge blanking time.

In addition, there is a maximum on time, t_{OnMax}, limitation implemented in the IC. Once the gate drive has been in high state longer than the maximum on time, it will be turned off to prevent the switching frequency from going too low because of long on time.

4.4 Current Limitation

There is a cycle by cycle current limitation realized by the current limit comparator to provide an overcurrent detection. The source current of the MOSFET is sensed via a sense resistor RCS. By means of RCS the source current is transformed to a sense voltage V_{CS} which is fed into the pin CS. If the voltage V_{CS} exceeds an internal voltage limit, adjusted according to the Mains voltage, the comparator immediately turns off the gate drive.

To prevent the Current Limitation process from distortions caused by leading edge spikes, a Leading Edge Blanking time (t_{LEB}) is integrated in the current sensing path.

A further comparator is implemented to detect dangerous current levels (V_{CSSW}) which could occur if one or more transformer windings are shorted or if the secondary diode is shorted. To avoid an accidental latch off, a spike blanking time of tCSSW is integrated in the output path of the comparator.

4.4.1 Foldback Point Correction

When the main bus voltage increases, the switch on time becomes shorter and therefore the operating frequency is also increased. As a result, for a constant primary current limit, the maximum possible output power is increased, which the converter may have not been designed to support.

To avoid such a situation, the internal foldback point correction circuit varies the V_{CS} voltage limit according to the bus voltage. This means the V_{CS} will be decreased when the bus voltage increases. To keep a constant maximum input power of the converter, the required maximum V_{CS} versus various input bus voltage can be calculated, which is shown in **Figure 6**.

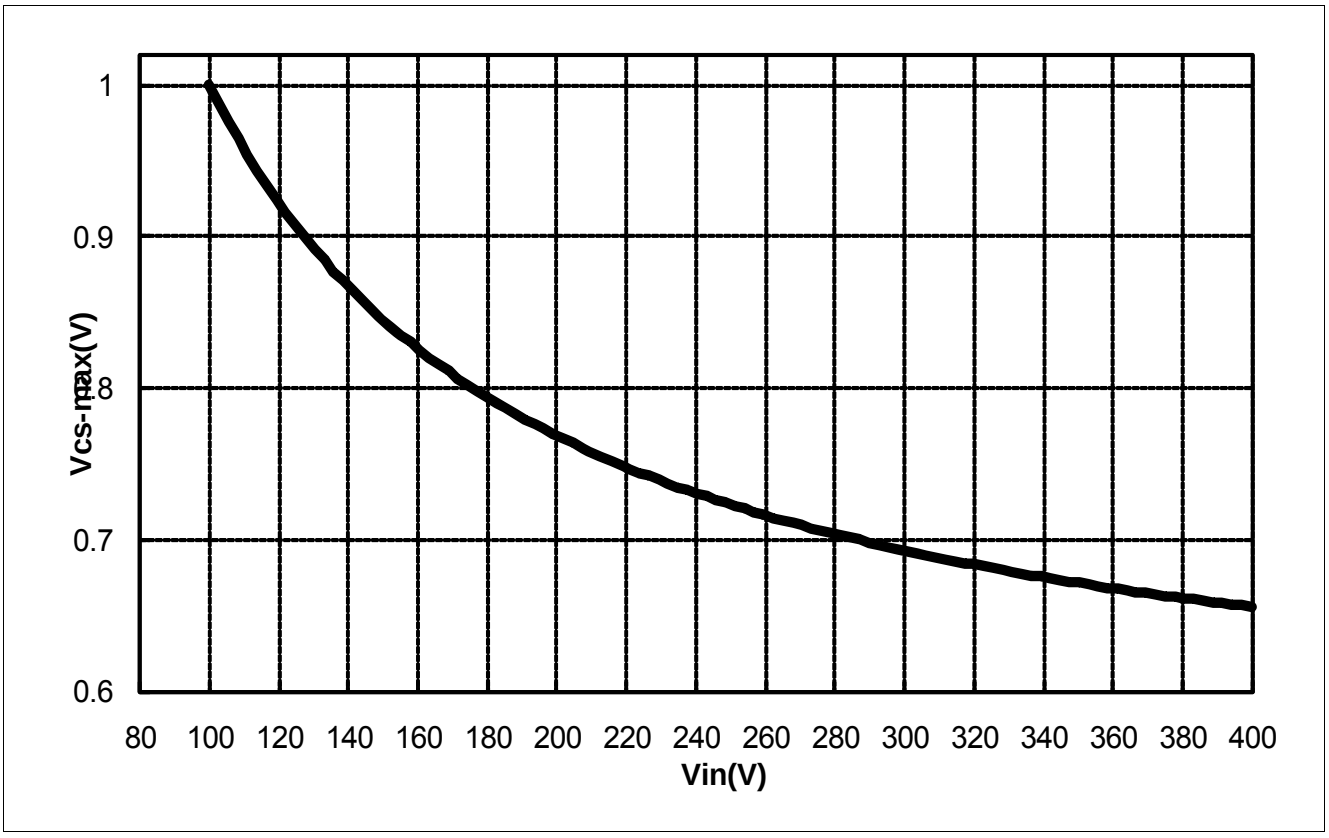


Figure 6 Variation of the VCS limit voltage according to the IZC current

According to the typical application circuit, when MOSFET is turned on, a negative voltage proportional to bus voltage will be coupled to auxiliary winding. Inside ICL8002G, an internal circuit will clamp the voltage on ZC pin to nearly 0 V. As a result, the current flowing out from ZC pin can be calculated as

$$I_{ZC} = \frac{V_{BUS} N_a}{R_{ZC\_1} N_P} \quad (5)$$

When this current is higher than IZC_1, the amount of current exceeding this threshold is used to generate an offset to decrease the maximum limit on VCS. Since the ideal curve shown in **Figure 6** is a nonlinear one, a digital block in ICL8002G is implemented to get a better control of maximum output power. Additional advantage to use digital circuit is the production tolerance is smaller compared to analog solutions. The typical maximum limit on VCS versus the ZC current is shown in **Figure 7**.

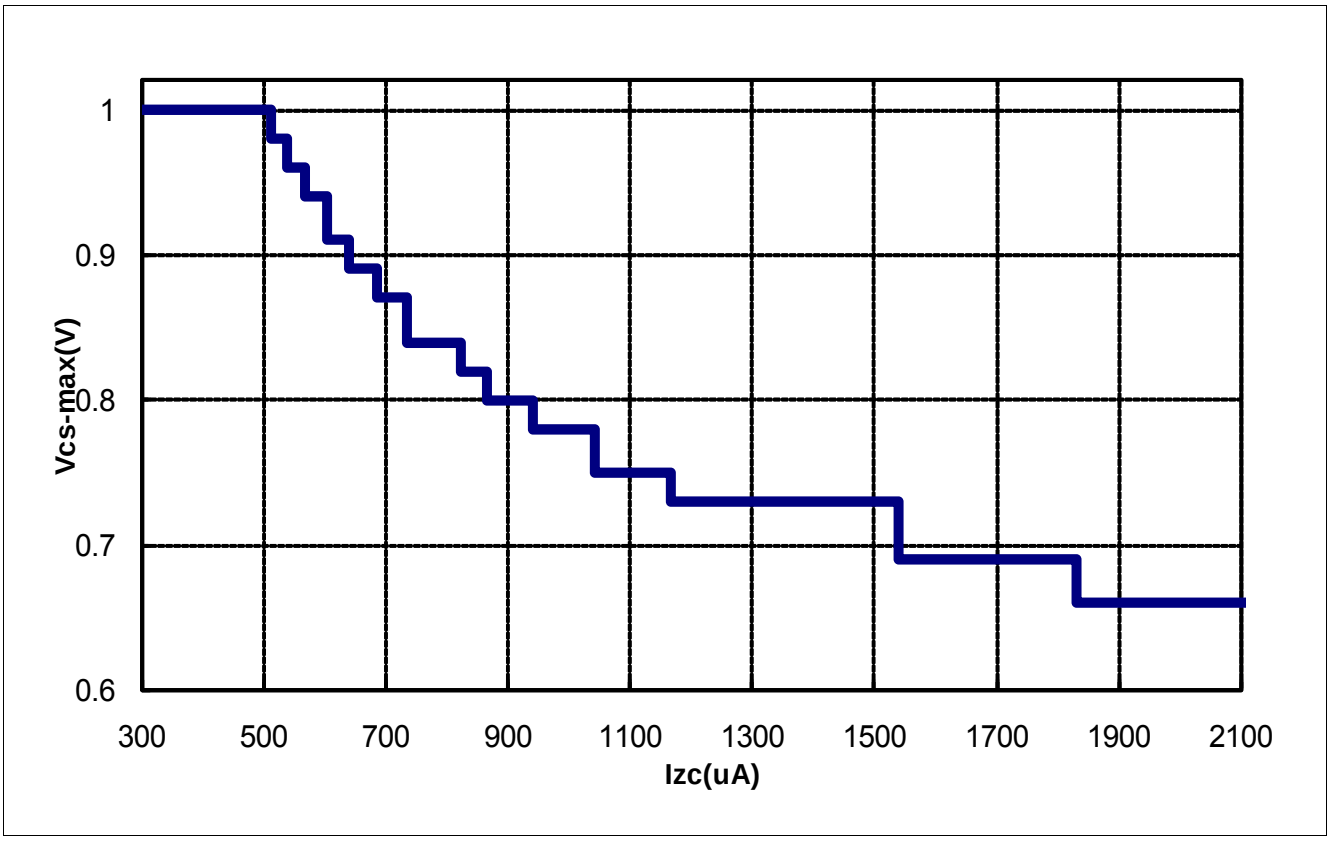


Figure 7 VCS-max versus IZCi

4.4.2 Additonal Features in ICL8002G compare to ICL8001G

1) New Valley Switching Sheme which minimizes light shimmer effect.

2) Helps for the continous dimming curve for smooth dimming.

3) Internal hold-up resistor value has been increased for better shaping of the input current.

4) Better shaping of the input current results in high PFC and stable dimming at higher LED current precision.

5) Better PFC leads to lower THD operation to meet the EN standards for hormonics.

4.5 iProtection Functions

The IC provides full protection functions. The following table summarizes these protection functions.

Table 2 Protection features

VCC Overvoltage	Auto Restart Mode
VCC Undervoltage	Auto Restart Mode
Over temperature	Auto Restart Mode
Output Overvoltage	Latched Off Mode
Short Winding	Latched Off Mode

During operation, the VCC voltage is continuously monitored. In case of an under- or an over-voltage, the IC is reset and the main power switch is then kept off. After the VCC voltage falls below the threshold V_{VCCoff}, the startup cell is activated. The VCC capacitor is then charged up. Once the voltage exceeds the threshold V_{VCCon}, the IC begins to operate with a new soft-start.

During off-time of the power switch, the voltage at the zero-crossing pin is monitored for output over-voltage detection. If the voltage is higher than the preset threshold V_{ZCOVP}, the IC is latched off after the preset blanking time.

There is also the overvoltage protection being implemented at VR, when this voltage exceeds V_{VROVP}, the device goes into Auto Restart Mode.

If the junction temperature of IC exceeds 140 ^{0}C, the IC enter into autorestart mode.

If the voltage at the current sensing pin is higher than the preset threshold V_{CSSW} during on-time of the power switch, the IC is latched off. This is short-winding protection.

During latch-off protection mode, when the VCC voltage drops to 10.5 V,the startup cell is activated and the VCC voltage is charged to 18 V then the startup cell is shut down again and repeats the previous procedure.

There is also a maximum on time limitation inside ICL8002G. Once the gate voltage is high longer than t_{OnMAx}, it is turned off immediately.

5 Electrical Characteristics

Note: All voltages are measured with respect to ground (Pin 8). The voltage levels are valid if other ratings are not violated.

5.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 7 (V_{CC}) is discharged before assembling the application circuit.

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
HV Voltage	V_{HV}	–	500	V	
VCC Supply Voltage	V_{VCC}	-0.3	27	V	
VR Voltage	V_{VR}	-0.3	5.0	V	
ZCV Voltage	V_{ZC}	-0.3	5.0	V	
CS Voltage	V_{CS}	-0.3	5.0	V	
GD Voltage	V_{OUT}	-0.3	27	V	
Maximum current out from ZC pin	I_{ZCMAX}	3	–	mA	
Junction Temperature	T_J	-40	150	°C	
Storage Temperature	T_S	-55	150	°C	
Thermal Resistance Junction - Ambient	R_{thJA}	–	185	K/W	PG-DSO-8
ESD Capability (incl. Drain Pin)	V_{ESD}	–	2	kV	Human body model[1)]

1) According to EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5 kOhm series resistor).

5.2 Operating Range

Note: Within the operating range the IC operates as described in the functional description.

Table 4 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCC Supply Voltage	V_{VCC}	V_{VCCoff}	–	V_{VCCOP}	V	
Junction Temperature of Controller	Tj_{CON}	-25	–	130	°C	Tj_{CON}<T_J , Limited by over temperature protection

5.3 Characteristics

5.3.1 Supply Section

Note: The electrical characteristics involve the spread of values within the specified supply voltage and junction temperature range T_J from – 25 °C to 130 °C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V_{CC} = 18 V is assumed.

Table 5 Supply Section

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Start Up Current	$I_{VCCstart}$	–	300	550	µA	V_{VCC}= V_{VCCon}-0.2 V
VCC Charge Current	$I_{VCCcharge1}$	–	5.0	–	mA	V_{VCC}= 0 V
	$I_{VCCcharge2}$	0.8		–	mA	V_{VCC}= 1 V
	$I_{VCCcharge3}$	–	1.0	–	mA	V_{VCC}= V_{VCCon}-0.2 V
Maximum Input Current ofStartup Cell and CoolMOS®	$I_{DrainIn}$	–	–	2	mA	V_{VCC}= V_{VCCon}-0.2 V
Leakage Current ofStartup Cell	$I_{StartLeak}$	–	0.2	50	µA	V_{HV} = 610 V at T_j= 100°C
Supply Current in normal operation	I_{VCCNM}	–	1.5	2.3	mA	V_{VR}= 0 V and no switching
Supply Current in Auto Restart Mode with Inactive Gate	I_{VCCAR}	–	300	–	µA	I_{VR} = 0 A
Supply Current in Latch-off Mode	$I_{VCClatch}$	–	300	–	µA	
VCC Turn-On Threshold	V_{VCCon}	17.0	18.0	19.0	V	
VCC Turn-Off Threshold	V_{VCCoff}	9.8	10.5	11.2	V	
VCC Turn-On/Off Hysteresis	V_{VCChys}	–	7.5	–	V	

5.3.2 Internal Voltage Reference

Table 6 Internal Voltage Reference

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Internal Reference Voltage	V_{REF}	4.80	5.00	5.20	V	Measured at pin VR I_{VR} = 0

5.3.3 PWM Section

Table 7 PWM Section

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VR Refrence Pull-Up Resistor	R_{VR}	76	100	150	kΩ	
PWM-OP Gain	G_{PWM}	3.23	3.3	3.33	–	
Offset for Voltage Ramp	V_{PWM}	0.636	0.7	0.786	V	
Maximum on time in normal operation	t_{OnMax}	22	30	41	µs	

5.3.4 Current Sense

Table 8 Current Sense

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Peak current limitation in normal operation	V_{CSth}	0.97	1.03	1.09	V	
Leading Edge Blanking time	t_{LEB}	200	330	460	ns	

5.3.5 Soft Start

Table 9 Soft Start

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Soft-Start time	t_{SS}	8.5	12	–	ms	
Soft-start time step	t_{SS_S} 1)	–	3	–	ms	
Internal regulation voltage at first step	V_{CSth} 1)	–	1.76	–	V	
Internal regulation voltage step at soft start	V_{CSth} 1)	–	0.56	–	V	

1) The parameter is not subjected to production test - verified by design/characterization

5.3.6 Foldback Point Correction

Table 10 Foldback Point Correction

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ZCV current first step threshold	I_{ZC_FS}	0.35	0.5	0.621	mA	
ZCV current last step threshold	I_{ZC_LS}	1.3	1.7	2.2	mA	
CS threshold minimum	V_{CSMF}	–	0.66	–	V	I_{ZC} = 2.2 mA, V_{VR} = 3.8 V

5.3.7 Zero Crossing

Table 11 Zero Crossing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Zero crossing threshold voltage	V_{ZCCT}	50	100	170	mV	
Ringing suppression threshold	V_{ZCRS}	–	0.7	–	V	
Minimum ringing suppression time	t_{ZCRS1}	1.62	2.5	4.5	µs	$V_{ZC} > V_{ZCRS}$
Maximum ringing suppression time	t_{ZCRS2}	–	25	–	µs	$V_{ZC} < V_{ZCRS}$
Maximum restart time in normal operation	t_{OffMax}	30	42	57.5	µs	

5.3.8 Protection

Table 12 Protection

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCC overvoltage threshold	V_{VCCOVP}	24.0	25.0	26.0	V	
Output Overvoltage detection threshold at the ZCV pin	V_{ZCOVP}	3.55	3.7	3.84	V	
Overvoltage protection threshold at the VR pin	V_{VROVP}		4.5		V	
Overvoltage protection threshold Blanking time at VR pin	t_{OVP_B}	20	30	44	ms	
Blanking time for Output Overvoltage protection	t_{ZCOVP}	–	100	–	µs	
Threshold for short winding protection	V_{CSSW}	1.63	1.68	1.78	V	
Blanking time for short-windding protection	t_{CSSW}	–	190	–	ns	
Over temperature protection[1)]	T_{jCon}	130	140	150	°C	

1) The parameter is not subjected to production test - verified by design/characterization

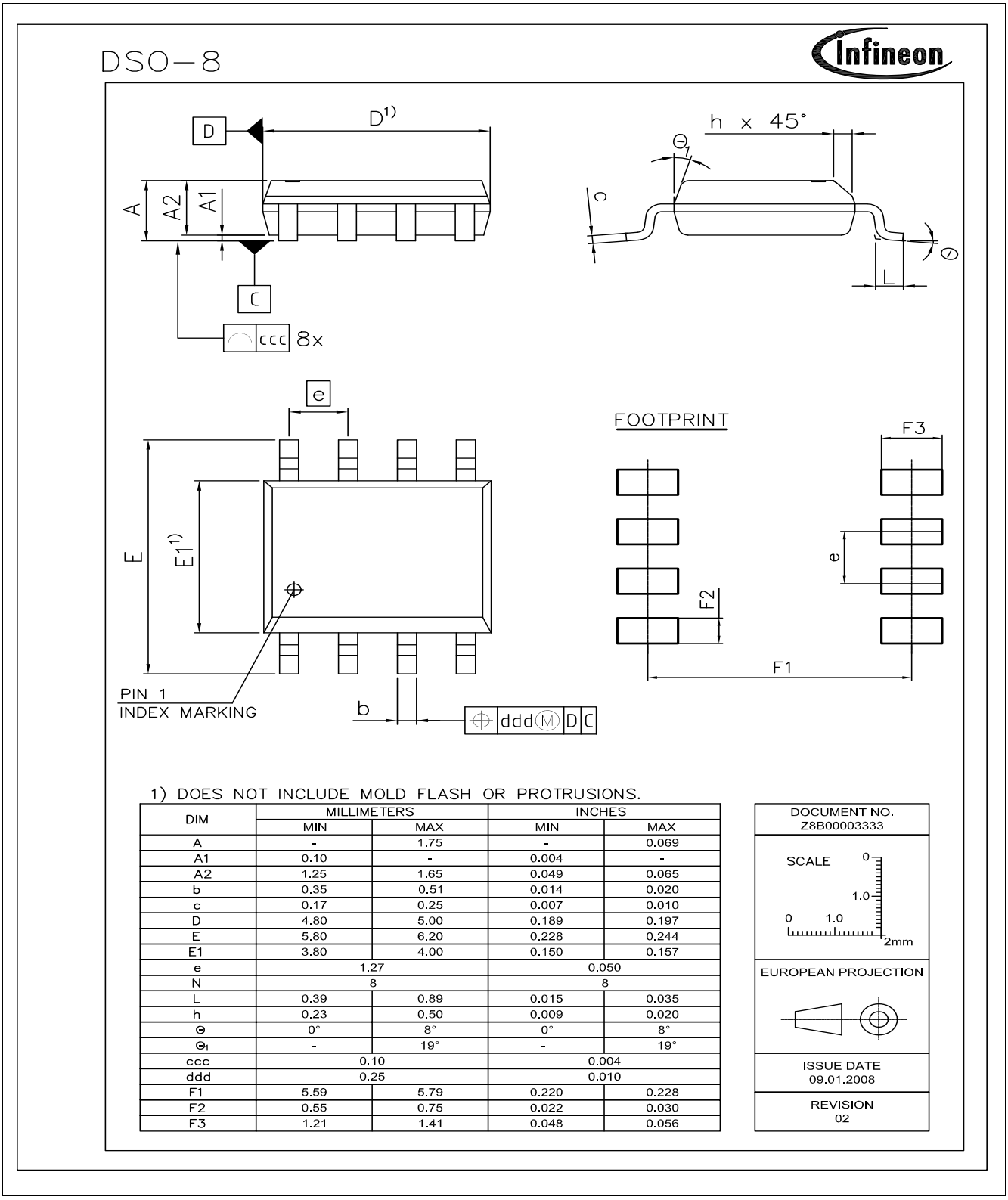
Note: The trend of all the voltage levels in the Control Unit is the same regarding the deviation except VVCCOVP

5.3.9 Gate Drive

Table 13 Gate Drive

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output voltage at logic low	$V_{GATElow}$	–	–	1.0	V	V_{VCC} = 18 V I_{OUT} = 10 mA
Output voltage at logic high	$V_{GATEhigh}$	9.0	10.0	–	V	V_{VCC} = 18 V I_{OUT} = -10 mA
Output voltage active shut down	$V_{GATEasd}$	–	–	1.0	V	V_{VCC} = 7 V I_{OUT} = 10 mA
Rise Time	t_{rise}	–	117	–	ns	C_{OUT} = 1.0 nF V_{GATE} = 2 V ... 8 V
Fall Time	t_{fall}	–	27	–	ns	C_{OUT} = 1.0 nF V_{GATE} = 8 V ... 2 V

6 Outline Dimension



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	-	0.004	-
A2	1.25	1.65	0.049	0.065
b	0.35	0.51	0.014	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27		0.050	
N	8		8	
L	0.39	0.89	0.015	0.035
h	0.23	0.50	0.009	0.020
Θ	0°	8°	0°	8°
Θ1	-	19°	-	19°
ccc	0.10		0.004	
ddd	0.25		0.010	
F1	5.59	5.79	0.220	0.228
F2	0.55	0.75	0.022	0.030
F3	1.21	1.41	0.048	0.056

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SCALE 0 1.0 0 1.0 2mm

EUROPEAN PROJECTION

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02

Figure 8 PG-DSO-8 (Pb-free lead plating Plastic Dual Small Outline)

Dimensions in mm.

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