Off-Line Digital Constant-Voltage LED Driver with Power Factor Correction

1.0 Features

- All-in-one low-cost off-line high power factor (PF) constant voltage (CV) controller supports fly-back, buck-boost, and buck topologies in isolated or non-isolated designs
- Supports universal AC input ($90V_{AC}$ – $277V_{AC}$) and DC input
- Primary-side control achieves very tight line and load regulation (±3%)
- Enhanced MOSFET driver supports output power up to 80W or above in a tiny SOT-23 package
- PF > 0.9 and THD < 20% across 50% to 100% output power range
- User-configurable minimum switching frequency (600Hz/1kHz) ensures no-load standby power consumption < 200mW or below
- Internal loop compensation ensures stable operation with different types of loads: down-stream DC-DC converter, constant current (CC) load, LED load, and constant resistive (CR) load
- Supports wide range of output capacitance (with output voltage ripple ranging from 1% to 20% at full load)
- Adaptively adjusted output voltage limits accommodating different load conditions ensures <10% overshoot and undershoot for any load transient
- User-configurable maximum PWM switching frequency (90kHz or 120kHz)
- Built-in soft-start achieves fast and smooth start-up for all different operating conditions
- Active start-up scheme enables fastest possible start-up
- Built-in single-point fault protection features: output over-load, output over-voltage, output short and input voltage under-voltage protections
- Built-in over-temperature protection
- No audible noise over entire operating range

2.0 Description

The iW3627 is a high-performance single-stage AC/DC constant voltage (CV) controller with high power factor correction. It supports most commonly used isolated and non-isolated topologies including fly-back, buck-boost, and buck. The device operates at constant on-time mode to achieve high power factor (>0.9) across wide load range from full-load down to half-load (or lower). It can achieve excellent output voltage regulation over line and load variation without the need for secondary feedback circuit. It also eliminates the need for external loop compensation while maintaining stability over all operating conditions with different types of loads, including down-stream DC-DC converter, constant current (CC) load, LED load, and constant resistive (CR) load. The proprietary technique that adaptively adjusts output voltage limits to accommodate and undershoot for any load transient. The iW3627 operates in pulse-frequency-modulation (PFM) mode at light load to eliminate audible noise and meanwhile to achieve less than 200mW no-load standby power consumption.

Dialog's innovative proprietary technology maximizes the iW3627 performance in a tiny SOT-23 package. The iW3627 offers two multi-function pins allowing users to configure maximum and minimum switching frequencies with no cost or size impact, thereby providing design flexibility. In addition to providing input voltage sensing for input under-voltage protection, the V_{IN} pin also enables active start-up scheme to achieve the shortest possible start-up time without sacrificing active efficiency.

3.0 Applications

- Smart LED lighting
- LED lighting ballast
- Front-end pre-regulator

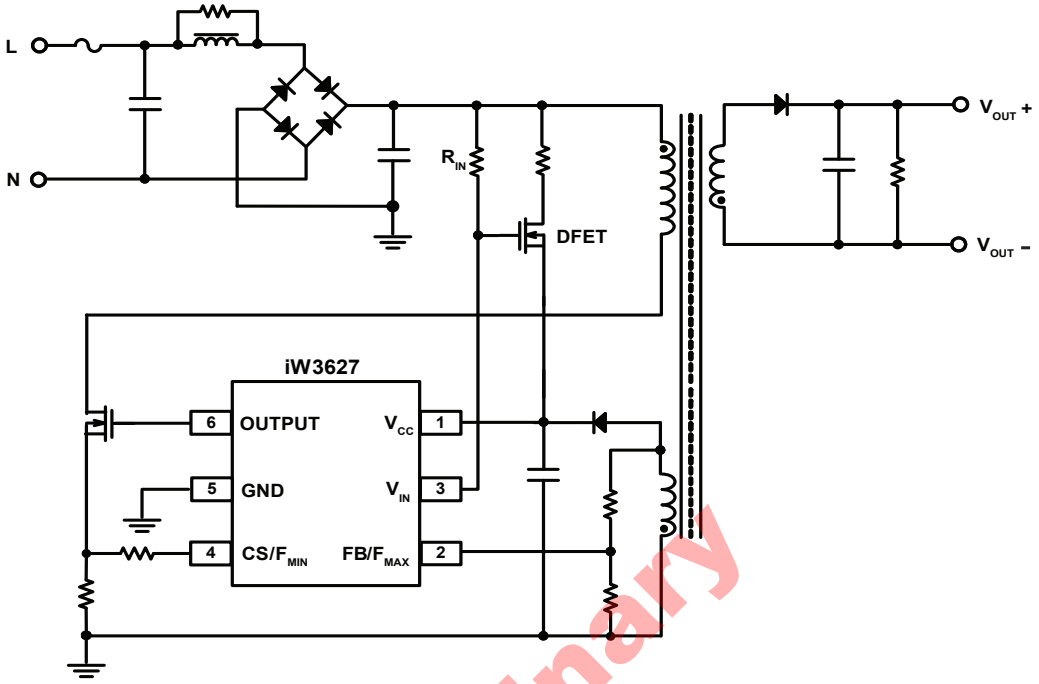


Figure 3.1: iW3627 Typical Application Circuit (Isolated Flyback Application)

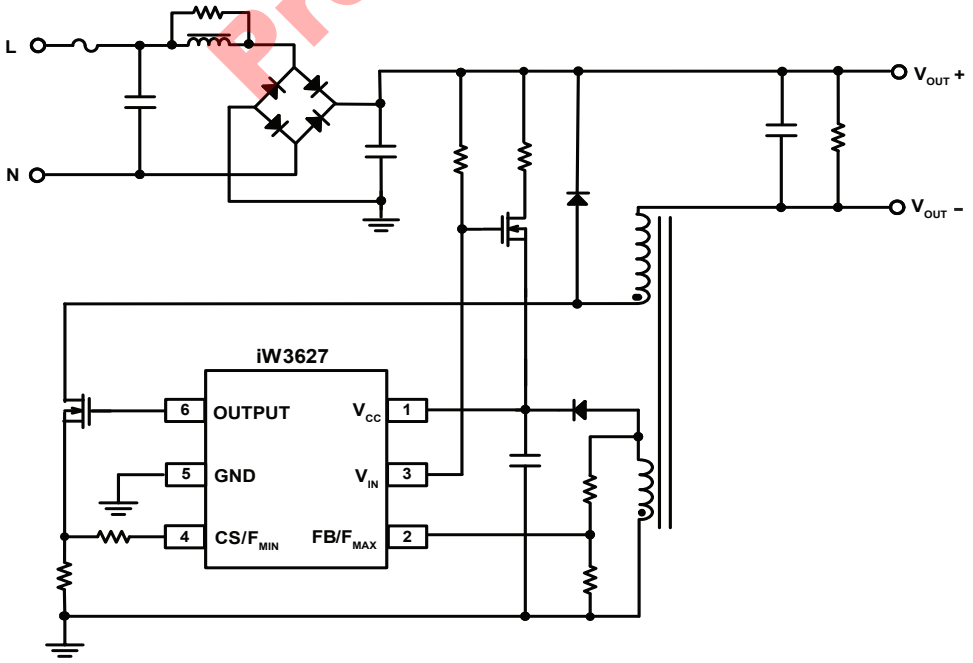


Figure 3.2: iW3627 Typical Application Circuit (Buck Application)

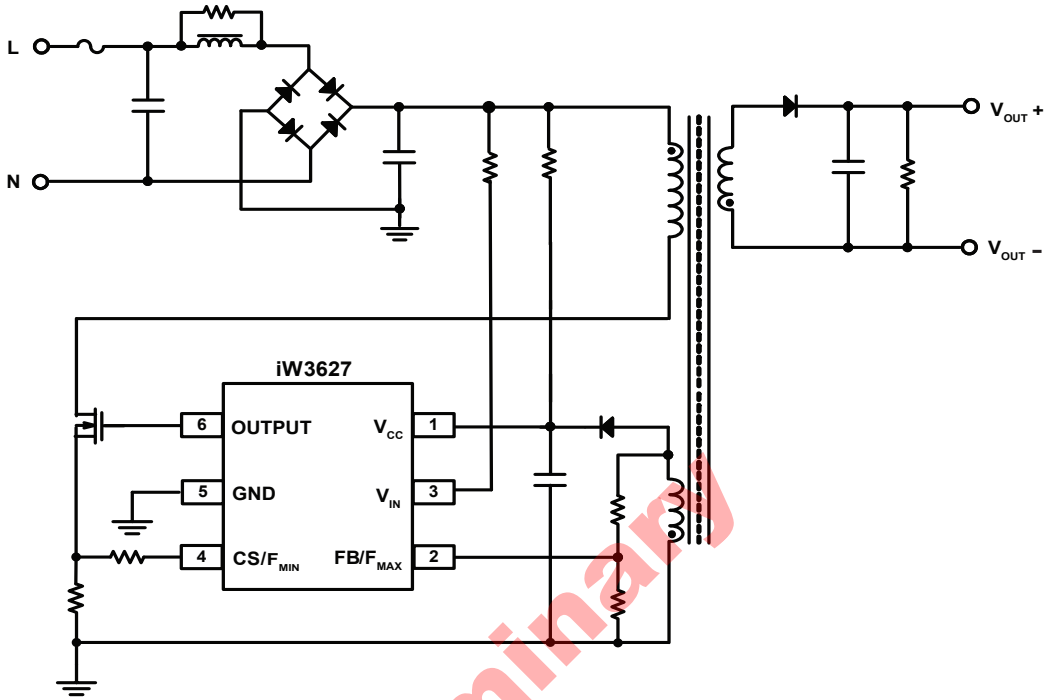


Figure 3.3: iW3627 Typical Application Circuit (Isolated Flyback Application Without Using Active Start-up Device)

4.0 Pinout Description

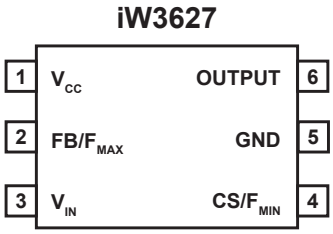


Figure 4.1: 6-Lead SOT-23 Package

Pin #	Name	Type	Pin Description
1	V_{CC}	Power Input	Power supply to control logic and MOSFET drive.
2	FB/F_{MAX}	Analog Input	Multi-function pin. Used to configure maximum switching frequency (F_{MAX}), and to enable/disable over-load protection (OLP) at the beginning of start-up. It also provides output voltage sense for primary regulation during normal operation.
3	V_{IN}	Analog Input	Multi-function pin. Used to control active start-up device and sense line voltage.
4	CS/F_{MIN}	Analog Input	Multi-function pin. Used to configure minimum switching frequency (F_{MIN}) at the beginning of the start-up. It also provides primary current sense for peak current detection and OCP protection.
5	GND	Ground	Ground.
6	OUTPUT	Output	Gate drive for external MOSFET switch.

5.0 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded.

Parameter	Symbol	Value	Units
DC supply voltage range (pin 1, I_{CC} = 20mA max)	V_{CC}	-0.3 to 18.0	V
Continuous DC supply current at V_{CC} pin (V_{CC} = 15V)	I_{CC}	20	mA
V_{IN} (pin 3)		-0.3 to 18.0	V
OUTPUT (pin 6)		-0.3 to 18.0	V
FB/F_{MAX} input (pin 2, $I_{FB/OTP}$ ≤ 10mA)		-0.7 to 4.0	V
CS/F_{MIN} input (pin 4)		-0.3 to 4.0	V
Maximum junction temperature	T_{JMAX}	150	°C
Operating junction temperature	T_{JOPT}	-40 to 150	°C
Storage temperature	T_{STG}	-65 to 150	°C
Thermal resistance junction-to-ambient	θ_{JA}	190	°C/W
ESD rating per JEDEC JESD22-A114		±2,000	V
Latch-up test per JESD78A		±100	mA

6.0 Electrical Characteristics

V_{CC} = 12V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
FB/F_{MAX} SECTION (Pin 2)						
Input leakage current	I_{BVS}	FB/F_{MAX} = 2V			1	µA
Nominal voltage threshold	$FB_{(NOM)}$	T_A=25°C, negative edge	1.521	1.536	1.551	V
Output OVP threshold	$FB_{(OVP)}$	T_A=25°C, negative edge		2		V
CS/F_{MIN} SECTION (Pin 4)						
Overcurrent threshold	V_{OCP}			1.15		V
CS/F_{MIN} regulation upper limit	$V_{IPK(HIGH)}$			0.9		V
CS/F_{MIN} regulation lower limit (Note 3)	$V_{IPK(LOW)}$			0.16/0.2		V
Input leakage current	I_{LK}	CS/F_{MIN} = 0.9V			1	µA
OUTPUT SECTION (Pin 6)						
Driver pull-down ON-resistance	$R_{DS(ON)PD}$			6		Ω
Driver pull-up ON-resistance (Note 2)	$R_{DS(ON)PU}$			16/64		Ω
Maximum switching frequency (Note 3)	f_{SW_MAX}			90/120		kHz
Minimum switching frequency (Note 3)	f_{SW_MIN}			0.6/1.0		kHz
V_{CC} SECTION (Pin 1)						
Maximum operating voltage (Note 1)	$V_{CC(MAX)}$				18	V
Start-up threshold	$V_{CC(ST)}$	V_{CC} rising		14.5		V
Undervoltage lockout threshold	$V_{CC(UVL)}$	V_{CC} falling		6.5		V
Start-up current	$I_{IN(ST)}$	V_{CC} = 10V		1.0		µA
Quiescent current	I_{CCQ}	V_{CC} = 14V, without driver switching		1.7		mA
Zener breakdown voltage	V_{ZB}	Zener current = 5mA T_A=25°C		19.5		V
V_{IN} SECTION (Pin 3)						
Maximum operating voltage (Note 1)	$V_{MULTI(MAX)}$				18	V
Brown-in voltage	V_{BRN_IN}			0.332		V

Electrical Characteristics (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Brown-out voltage	V_{BRN_OUT}			0.293		V
V_{IN} internal resistor	Z_{VIN}			12.5		kΩ

Notes:

Note 1: These parameters are not 100% tested. They are guaranteed by design and characterization. Refer to Section 9.0 for operation details.

Note 2: This parameter is determined by IC options. See Section 11.0 for details.

Note 3: This parameter is determined by configuration resistors at CS/F_{MIN} or FB/F_{MAX} pin. See Section 9.3 for details.

7.0 Typical Performance Characteristics

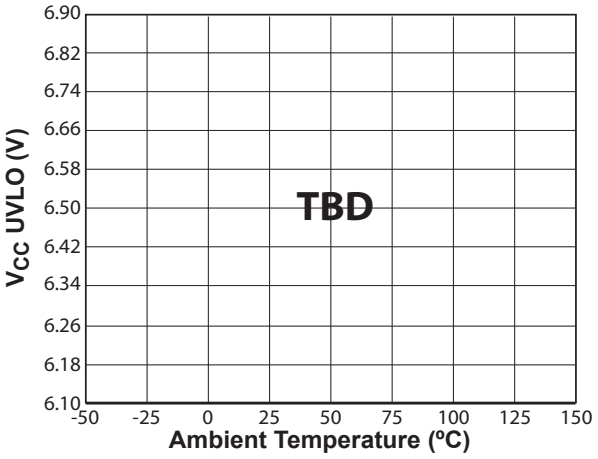


Figure 7.1 : V_{CC} UVLO vs. Temperature

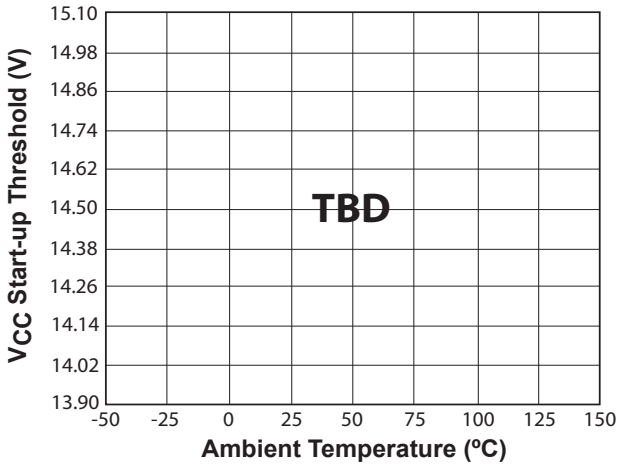


Figure 7.2 : Start-up Threshold vs. Temperature

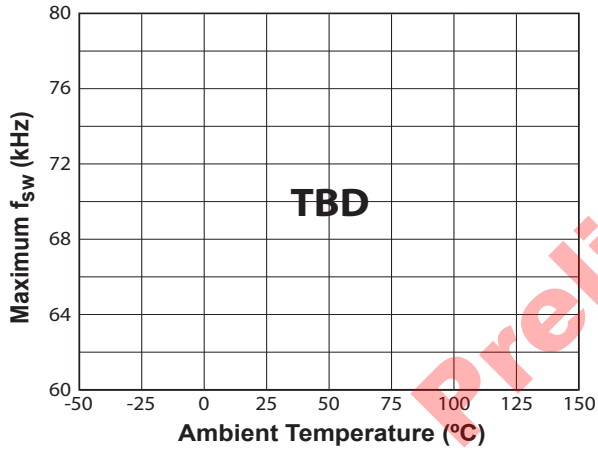


Figure 7.3 : Switching Frequency vs. Temperature[1]

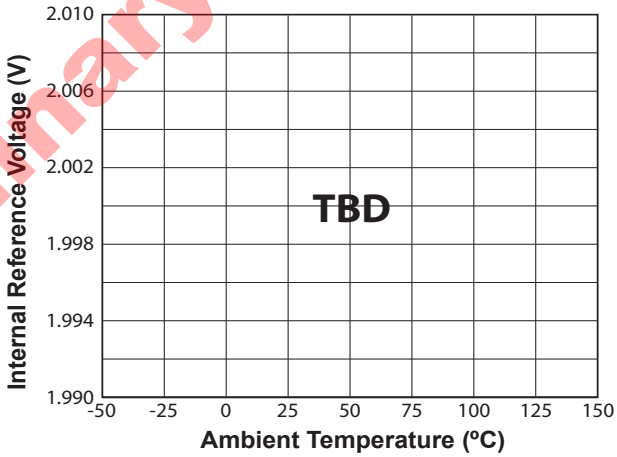


Figure 7.4 : Internal Reference vs. Temperature

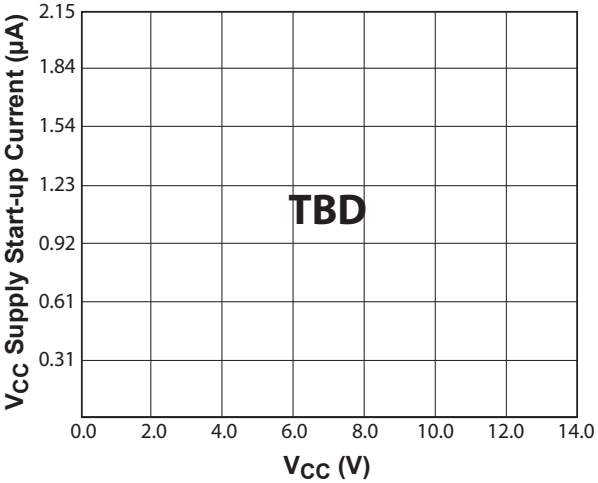


Figure 7.5 : V_{CC} vs. V_{CC} Supply Start-up Current

Notes:

Note 1. Operating frequency varies based on the operating conditions; see Section 9.7 for more details.

8.0 Functional Block Diagram

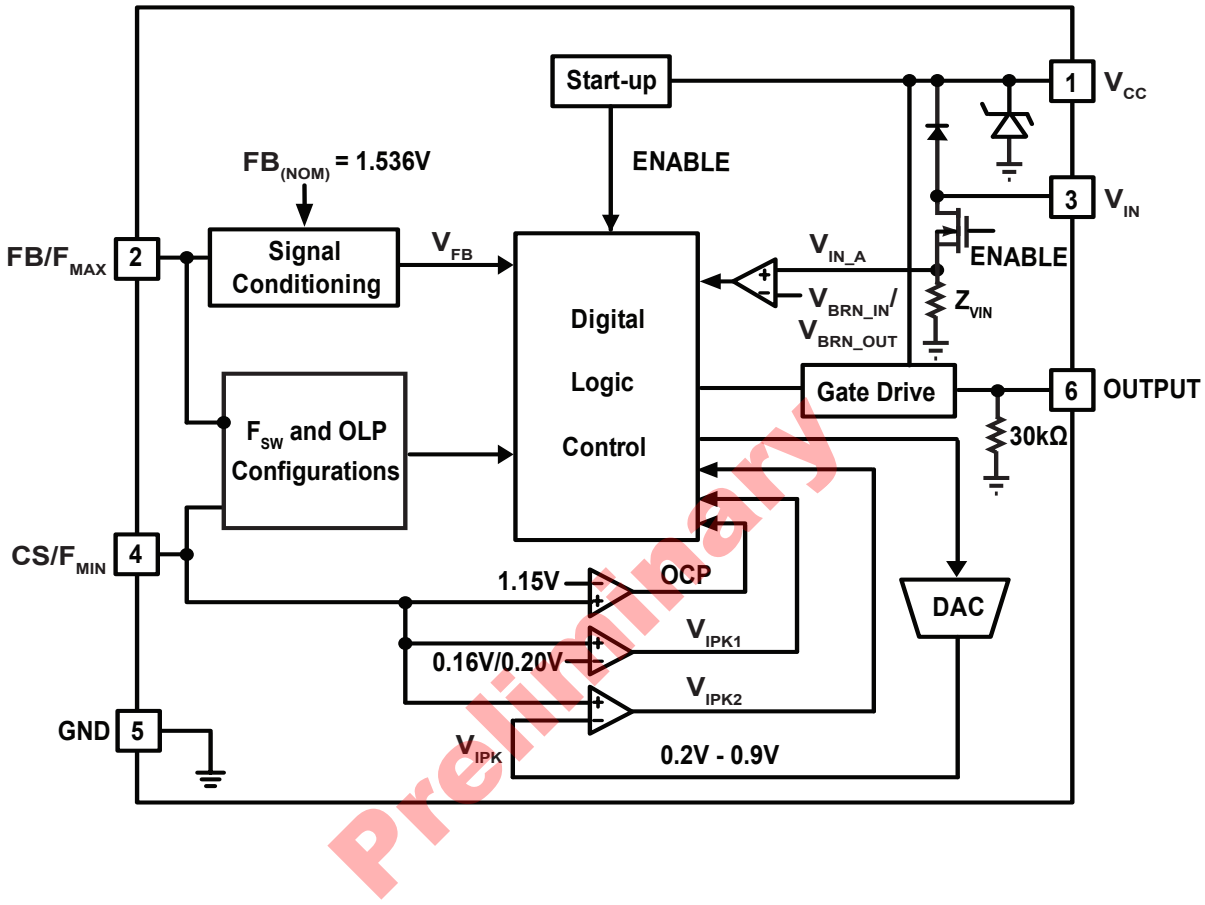


Figure 8.1: iW3627 Functional Block Diagram

9.0 Theory of Operation

The iW3627 is a digital power controller dedicated for single-stage off-line constant voltage LED driver with power factor correction. The device uses a new, proprietary primary-side control technology to eliminate the opto-isolated feedback and secondary regulation circuits required in traditional designs. This results in a low-cost small-size solution for LED lighting applications. The core switching processor uses fixed frequency Pulse-Width-Modulation (PWM) control and Discontinuous Conduction Mode (DCM) operation at high output power level and switches Pulse-Frequency-Modulation (PFM) control at light loads to maximize efficiency. Furthermore, Dialog's digital control technology enables fast and tight dynamic response, tight output regulation and full-featured circuit protection with primary side control.

The block diagram in Figure 8.1 shows that the iW3627 has CS/F_{MIN} and FB/F_{MAX} pins, each with two-fold functions. At the beginning of start-up, a fixed current source flows out of the two pins alternatively, resulting in generated voltage levels proportional to resistance values from the pins to GND, which are then identified by the controller to set the requirements for F_{MIN}, F_{MAX}, and OLP respectively. During a normal operation, the digital logic control block generates on-time and off-time information based on the FB/F_{MAX} signal and provides commands to dynamically control the external MOSFET gate voltage. The CS/F_{MIN} is an analog input configured to sense the primary current in a voltage form. In order to achieve a peak current mode control and cycle-by-cycle current limit, the controller compares the CS/F_{MIN} signal with two thresholds: $V_{IPK(HIGH)}$ (0.9V typical) and $V_{IPK(LOW)}$ (0.16V or 0.2V typical by IC options). The $V_{IPK(HIGH)}$ sets the maximum primary-side current value for OLP and the $V_{IPK(LOW)}$ sets the CS/F_{MIN} clamp voltage in PFM mode. The iW3627 uses an advanced digital control algorithm to reduce system design time and increase reliability. The system loop is automatically compensated internally by a digital error amplifier. Stability is guaranteed as the digital control loop dynamically adjusts parameters internally to maintain system phase margin > 45 degrees and gain margin > -20dB. No external analog components are required for loop compensation.

The iW3627 operates in quasi-resonant mode to provide high efficiency and simplify EMI design. In addition, the iW3627 incorporates a number of key built-in protection features, including output over-voltage protection (OVP), output short protection (OSP), output over-load protection (OLP), main power MOSFET over-current protection (OCP), input brown-out protection (BRP), and CS/F_{MIN} fault protection. Using Dialog's state-of-the-art primary-feedback technology, the iW3627 removes the need for secondary feedback circuit while achieving excellent line and load regulation.

9.1 Pin Detail

Pin 1 – V_{CC}

Power supply for the controller during normal operation. The controller starts up when V_{CC} voltage reaches 14.5V (typical) and shuts down when the V_{CC} voltage drops below 6.5V (typical) respectively. A decoupling capacitor of 0.1µF or so should be connected between the V_{CC} pin and GND.

Pin 2 – FB/F_{MAX}

Used to configure F_{MAX} setting and enable/disable OLP at the beginning of start-up. It is also used to sense output during a normal operation for output voltage regulation.

Pin 3 – V_{IN}

Input voltage sensing. This signal is pulled down and connected to an internal 12.5k (typical) resistor to sense the input voltage after power up ENABLE is high. It is also the control signal for the active start-up device. The active start-up device is cut off when V_{IN} is pulled low.

Pin 4 – CS/F_{MIN}

Used to configure F_{MIN} setting at the beginning of start-up. It is used to sense primary current during normal operation for cycle-by-cycle peak current control and limit.

Pin 5 – GND

Ground.

Pin 6 – OUTPUT

Gate drive for the external power FET switch.

9.2 Active Start-up and Adaptively Controlled Soft-Start

The iW3627 features a proprietary soft-start scheme to achieve fast yet smooth ramp-up of output voltage for a variety of output conditions including output voltage up to 100V above. In addition, the active start-up scheme enables shortest possible turn-on delay without sacrificing operating efficiency.

Refer to Figure 8.1 for the block diagram and Figure 3.1 for the active start-up circuit using external depletion NFET. Prior to start-up, the internal ENABLE signal is low, and the V_{IN} pin voltage closely follows the V_{CC} pin voltage, as

shown in Figure 9.1. Consequently, the depletion NFET is turned on, allowing the start-up current to charge the V_{CC} bypass capacitor. When the V_{CC} bypass capacitor is charged to a voltage higher than the start-up threshold $V_{CC(ST)}$, the ENABLE signal becomes active and activates the control logic. The V_{IN} is pulled down to ground through an internal resistor Z_{VIN}. The Z_{VIN} and the V_{IN} external resistor R_{IN} form a voltage divider to sense the input voltage. The scale-down input voltage is connected to the V_{IN_A} inside the IC. The iW3627 begins to perform an initial OTP check (See Section 9.12) followed by F_{MIN}/F_{MAX}/OLP configuration (See section 9.3). Afterwards, the control logic waits for about 500µs before starting an input voltage brown-out check. Once V_{IN_A} is higher than V_{BRN_IN}, the iW3627 begins a soft-start function. The whole soft-start process can break down into several stages based on the output voltage levels, which is indirectly sensed by the FB/F_{MAX} signal at the primary side. At different stages, the iW3627 adaptively controls the switching frequency and primary-side peak current such that the output voltage can always build up very fast at the early stages and smoothly transitions to the desired regulation voltage level, meanwhile meeting the power factor requirement at steady-state operation.

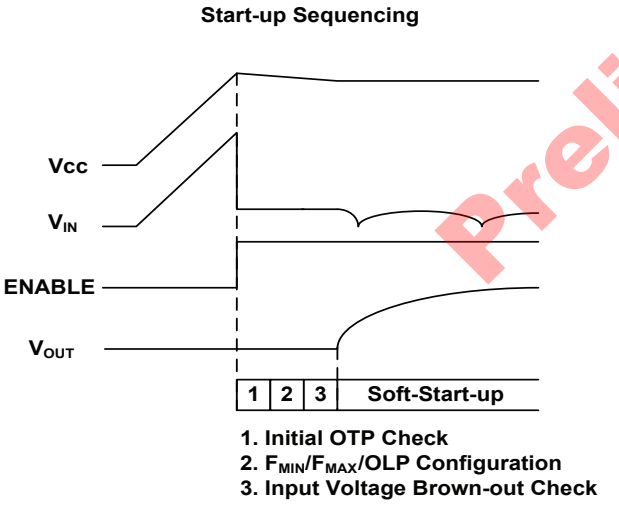


Figure 9.1: Start-up Sequencing Diagram

As the ENABLE signal initiates the control logic, it also pulls down the V_{IN} pin voltage at the same time, which turns off the depletion mode N-FET, thus eliminating the start-up resistors power consumption during a normal operation.

If at any time the V_{CC} voltage drops below the under-voltage lockout (UVLO) threshold $V_{CC(UVL)}$, then the iW3627 goes to shutdown. At this time the ENABLE signal becomes low, and the V_{CC} capacitor begins to charge up again towards the start-up threshold to initiate a new soft-start process.

In applications where the active start-up is not needed, the start-up resistor can be directly connected to the V_{CC} pin without using the active start-up device. Refer to Figure 3.3 for the application circuit.

9.3 F_{MAX}, F_{MIN}, and OLP Configurations

The iW3627 allows users to configure F_{MAX} and F_{MIN}, and to enable or disable OLP externally. In the iW3627, the PWM switching frequency F_{MAX} can be set to 90kHZ or 120kHz. It is recommended to choose 90kHz frequency for most applications since it is optimized for achieving high efficiency and small size. 120kHz frequency can be used in low power designs for minimal size. The PFM minimum frequency F_{MIN} can be set to 1kHz or 600Hz. Choose 1kHz frequency for better transient performance, and choose 600Hz frequency for minimal standby power. In addition, the OLP can also be enabled or disabled.

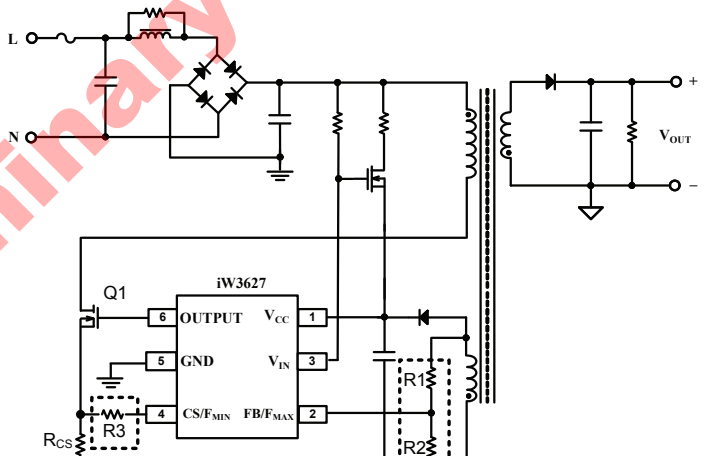


Figure 9.2: Typical Application Circuit Highlighting Configuration Resistors

The configurations of these parameters are only performed once after the ENABLE signal becomes active, and completed before the brown-out check begins. The configurations involve CS/F_{MIN} and FB/F_{MAX} pins and some resistors connected to the pins. Figure 9.2 shows the schematic highlighting the resistors used for configurations. During the F_{MIN} configuration, the iW3627 does not send out any drive signal at the OUTPUT pin, and the switch Q1 remains in off-state. A fixed current flows out of the CS/F_{MIN} pin, which generates a voltage proportional to the resistance value of R3 and R_{CS} (in series). The internal digital control block identifies the resistance value between CS/F_{MIN} pin and ground, and then sets the control algorithm accordingly. Table 9.1 lists the resistance range of R_3 for configuring the F_{MIN}.

The selection of R3 and R_{CS} is straight-forward. R_{CS} is usually small and its resistance is negligible compared to

R3 in determining F_{MIN} configuration. However, it directly sets peak primary current values for OLP and for entering PFM mode correspondingly, whereas R3 does not play a role. Therefore, the values of R3 and R_{CS} can be determined separately.

Following the completion of configuring F_{MIN}, the iW3627 enters the stage of configuring F_{MAX} and OLP selection. During this stage, switch Q1 still remains in off-state, and the fixed current flows out of the FB/F_{MAX} pin and generates a voltage proportional to the paralleled resistance of R1 and R2, since the bias winding is virtually shorted. Consequently, the paralleled resistance of R1 and R2 is identified and used to set the F_{MAX} and enable or disable OLP. Meanwhile, during normal operation, the FB/F_{MAX} pin reflects output voltage in real-time. The ratio of R1 to R2 sets nominal output voltage, which represents the voltage level the iW3627 attempts to regulate. Based on the two restrictions, R1 and R2 can be readily derived.

The iW3627 provides four sets of F_{MAX} and OLP options. Table 9.2 lists the resistance range of paralleled R1 and R2 for each configuration option.

9.4 Understanding Primary Feedback

Figure 9.3 illustrates a simplified flyback converter (a similar concept also applies to the buck-boost and buck converters). When the switch Q1 conducts during $t_{ON}(t)$, the current $i_g(t)$ is directly drawn from rectified sinusoid $v_g(t)$. The energy $E_g(t)$ is stored in the magnetizing inductance L_M. The rectifying diode D1 is reversely biased and the load current I_O is supplied by the secondary capacitor C_O. When Q1 turns off, D1 conducts and the stored energy in the inductor is delivered to the output.

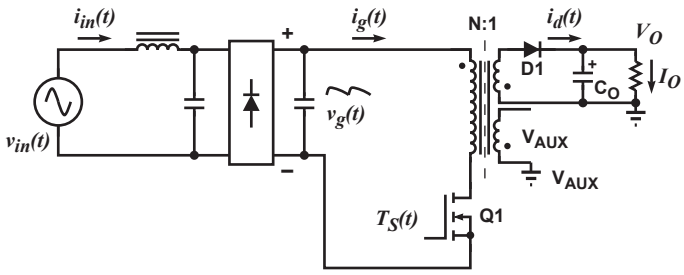


Figure 9.3: Simplified Flyback Converter

In order to tightly regulate the output voltage, the information about the output voltage and load current need to be accurately sensed. In the DCM flyback converter, this information can be read via the auxiliary winding or the primary magnetizing inductance (L_M). During the Q1 on-time, the load current is supplied from the output filter capacitor C_O. The voltage across L_M is $v_g(t)$, assuming the voltage dropped across Q1 is zero. The current in Q1 ramps up linearly at a rate of:

Table 9.1: Recommended Resistance Range to Set Minimum Switching Frequency (F_{MIN})

F_{MIN} Level	1	2
R3 Range* (kΩ)	0.1 - 0.85	1.2 – 1.55
F_{MIN} (kHz)	1	0.6

Table 9.2: Recommended Resistance Range to Set Maximum Switching Frequency and OLP Selection

Option Code	1	2	3	4
Paralleled R1 and R2 Range (kΩ)*	1.80 – 2.00	2.50 – 3.00	3.65 – 4.40	5.20 – 7.35
F_{MAX} (kHz)	90	120	90	120
OLP	Enable	Enable	Disable	Disable

**Using resistance out of the recommended range may affect voltage regulation performance.*

$$\frac{di_g(t)}{dt} = \frac{v_g(t)}{L_M} \quad (9.1)$$

At the end of on-time, the current has ramped up to:

$$i_{g\_peak}(t) = \frac{v_g(t) \times t_{ON}}{L_M} \quad (9.2)$$

This current represents a stored energy of:

$$E_g = \frac{L_M}{2} \times i_{g\_peak}(t)^2 \quad (9.3)$$

When Q1 turns off at t_O, $i_g(t)$ in L_M forces a reversal of polarities on all windings. Ignoring the communication-time caused by the leakage inductance L_K at the instant of turn-off t_O, the primary current transfers to the secondary at a peak amplitude of:

$$i_d(t) = \frac{N_P}{N_S} \times i_{g\_peak}(t) \quad (9.4)$$

Assuming the secondary winding is master, and the auxiliary winding is slave,

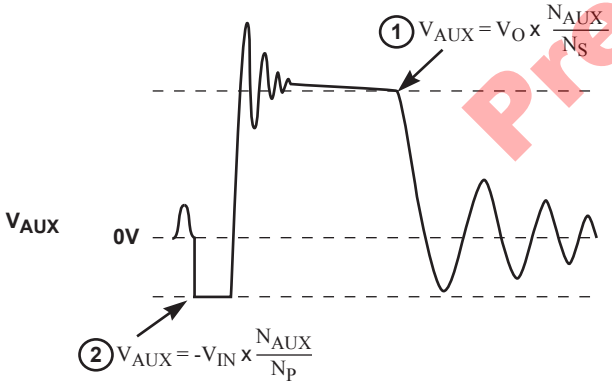


Figure 9.4: Auxiliary Voltage Waveforms

The auxiliary voltage is given by:

$$V_{AUX} = \frac{N_{AUX}}{N_S}(V_O + \Delta V) \quad (9.5)$$

and reflects the output voltage as shown in Figure 9.4.

The voltage at the load differs from the secondary voltage by a diode drop and IR losses. Thus, if the secondary voltage is always read at a constant secondary current, the difference between the output voltage and the secondary voltage is a fixed ΔV. Furthermore, if the voltage can be read when the secondary current is small, ΔV is also small. With the iW3627, ΔV can be ignored.

The real-time waveform analyzer in the iW3627 reads this information cycle by cycle. The part then generates a feedback voltage V_{FB}. The V_{FB} signal precisely represents the output voltage under most conditions and is used to regulate the output voltage.

9.5 Constant Voltage Operation

The iW3627 incorporates constant voltage (CV) operation, where the average of output voltage maintains constant by regulating the point 1 indicated in Figure 9.4 to $FB_{(NOM)}$ (1.536V typically). During a constant voltage operation, the iW3627 may operate in pulse-width-modulation (PWM) mode or pulse-frequency-modulation (PFM) mode, depending on the load conditions. In particular, the iW3627 allows the switching frequency to drop as low as 600Hz (or 1kHz by configuration options) at PFM mode, which helps the system stay regulated at very light load condition, thus improving the active operating efficiency by using a large pre-load resistor. The typical no-load standby power consumption is less than 200mW. No load standby power can be further minimized by removing the V_{IN} external sensing resistor and connecting a 100kΩ between the V_{IN} and V_{CC} pins, as shown in Figure 9.5.

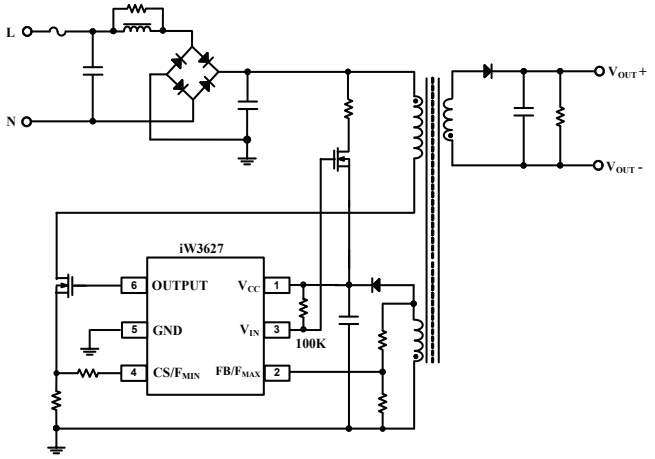


Figure 9.5: Minimizing No-Load Standby Power By Removing R_{IN} Resistor

For primary-side control, it is a big challenge to sense output voltage accurately when input voltage is near zero-crossing region, where stored transformer energy for each switching cycle is small and cannot ensure a good-quality sense signal from bias winding. This is especially true for buck converter

since there is a region during which the instantaneous input voltage is less than output voltage, therefore there is zero energy stored in the transformer and thus no well-sensed voltage signal is available in this region. The iW3627 adopts an innovative proprietary technique that recovers the output voltage information in these operating zones, and achieves super-tight output voltage regulation across the entire line and load ranges.

9.6 Adaptive Output Voltage Limit

For a single-stage operation, output voltage (V_{OUT}) ripple is related to output capacitance (C_{OUT}): lower C_{OUT} results in higher V_{OUT} ripple. For an electrolytic capacitor, C_{OUT} drops as it ages, which causes the V_{OUT} ripple to increase. In addition, the electrolytic capacitor can have a large capacitance tolerance (e.g. ±20%). Given the above factors, it is very difficult for the primary-side regulator to set a proper output transient detection criteria for accommodating these factors and respond fast. The iW3627 uses an innovative "adaptive output voltage limit" technique to well accommodate these factors to achieve fast and tight transient response at all work conditions.

The iW3627 first identifies the ripple voltage during normal operation, and then sets the maximum and minimum output limits slightly above or below the ripple accordingly (±5% – ±10%, adaptively adjusted to accommodate output voltage ripple change). In the case when the output limit is hit, the iW3627 determines a transient is occurring, it immediately boosts the loop bandwidth to recover the output voltage as fast as possible. With output limits adaptively changed according to load condition, the iW3627 can accommodate the output capacitance variation and keep a tight overshot/ under (<10% typical) across the whole load range

In the iW3627, the maximum limit is set to be ±22.5%, which is a hard limit. So care needs to be taken to select C_{OUT} to make sure the V_{OUT} ripple does not trigger this limit during normal operation.

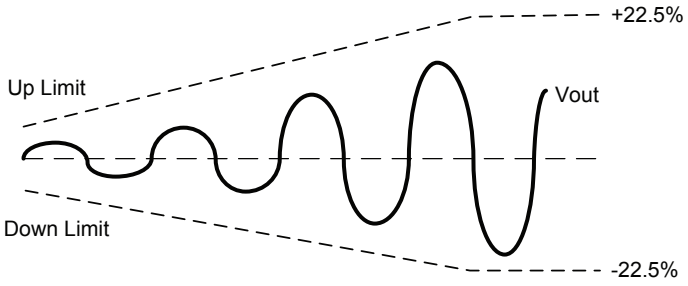


Figure 9.6: Adaptive Output Limit

Figure 9.6 shows the output limit (dashed curve) increases when output ripple increases and finally it clamps to +/-22.5%.

9.7 Variable Frequency Operation Mode

During each of the switching cycles, the falling edge of FB/F_{MAX} is checked. If the falling edge of FB/F_{MAX} is not detected, the off-time is extended until the falling edge of FB/F_{MAX} is detected. This results in the variable switching frequency operation. In particular, for low-line input voltage, the switch ON-time could be pushed relatively high, and in order to maintain DCM operation, the switching frequency cab drop much less than the normal 90kHz (or 120kHz, by configuration options). Additionally, the switching frequency in PFM mode can be pushed as low as 600Hz (or 1kHz by configuration options) at very light load to improve operating efficiency as well as to avoid audible noise.

9.8 Quasi-Resonant Switching

The iW3627 also incorporates a unique proprietary quasi-resonant switching scheme that achieves valley-mode turn on for every switching cycle. In valley mode switching, the MOSFET switch is turned on at the point where the resonant voltage across the drain and source of the MOSFET is at its lowest point (see Figure 9.7). By switching at the lowest V_{DS}, the switching loss is minimized.

Turning on at the lowest V_{DS} generates the lowest dV/dt, so the valley mode switching can also reduce EMI. Due to the nature of quasi-resonant switching, the actual switching frequency can vary slightly cycle by cycle, providing the additional benefit of reducing EMI.

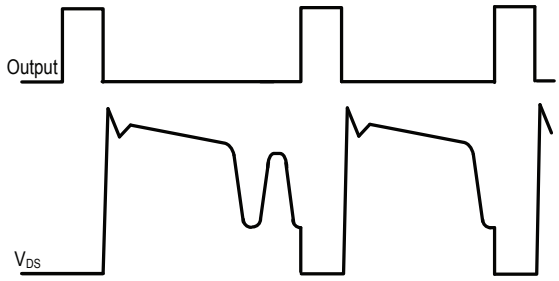


Figure 9.7: Valley Mode Switching

9.9 Internal Loop Compensation

The iW3627 incorporates an internal Digital Error Amplifier with no requirement for external loop compensation. It supports different kinds of load: CC load, down-stream DC-DC load, CR load, and LED load. For a typical power supply design, the loop stability is guaranteed to provide at least 45 degrees of phase margin and -20dB of gain margin.

9.10 Output Over-Voltage and Short Protections

The secondary maximum output voltage is limited by the iW3627. When the FB/F_{MAX} pin voltage exceeds the output OVP threshold ($FB_{(OVP)}$) in point 1 indicated in Fig. 9.4, the iW3627 shuts down.

Output short fault is also detected via the FB/F_{MAX} pin. When the point 1 in Figure 9.4 is below 115mV for several consecutive cycles, the iW3627 shuts down.

When any of these faults are met, the IC remains biased to discharge the V_{CC} supply. Once V_{CC} drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting start-up until the fault condition is removed.

9.11 PCL, OCP, OLP, and SRS Protections

Peak-current limit (PCL), over-current protection (OCP), over-load protection (OLP), and sense-resistor-short protection (SRSP) are features built into the iW3627. With the CS/F_{MIN} pin, the iW3627 is able to monitor the peak primary current. This allows for cycle-by-cycle peak current control and limit.

When the CS/F_{MIN} voltage (peak primary current multiplied by the CS/F_{MIN} resistor) reaches $V_{IPK(HIGH)}$ (0.9V typical), the output turns off immediately. If CS/PFM voltage reaches $V_{IPK(HIGH)}$ for more than 12.5% of the time in an half line cycle and the state lasts consecutively for about 500ms, over-load is detected and the iW3627 shuts down.

When the CS/F_{MIN} voltage is greater than 1.15V, over-current is detected and the IC immediately turns off the output driver until the next cycle. The output driver sends out a switching pulse in the next cycle, and the switching pulse continues if the OCP threshold is not reached; or, the switching pulse turns off again if the OCP threshold is reached. If the OCP occurs for several consecutive switching cycles, the iW3627 shuts down.

If the CS/F_{MIN} resistor is shorted, there is a potential danger that an over-current condition may not be detected. Therefore, the IC is designed to detect this sense-resistor-short fault during start-up and shut down immediately.

When any of these faults are met the IC remains biased to discharge the V_{CC} supply. Once V_{CC} drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting to start up until the fault condition is removed.

9.12 Internal OTP

The iW3627 incorporates an internal over-temperature protection (OTP). Before the soft-start process is initiated, the part first checks the junction temperature. If the junction temperature is above 125°C, then the system does not start up. Once the part starts up, the thermal shutdown temperature becomes 150°C. If the junction temperature reaches 150°C, OTP is triggered and IC shut down its OUTPUT. When OTP occurs, IC keeps biased to discharge V_{CC} supply. When the V_{CC} drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting start-up until the fault condition is removed.

9.13 Brown-Out Protection

The iW3627 also provides input under-voltage brown-out protection (BRP). After the ENABLE signal becomes high, the V_{IN} switch turns on and it is connected to V_{IN_A}. The V_{IN_A} is decided by

$$V_{IN\_A}=Z_{VIN}/(Z_{VIN}+R_{IN})*V_{BUS}$$

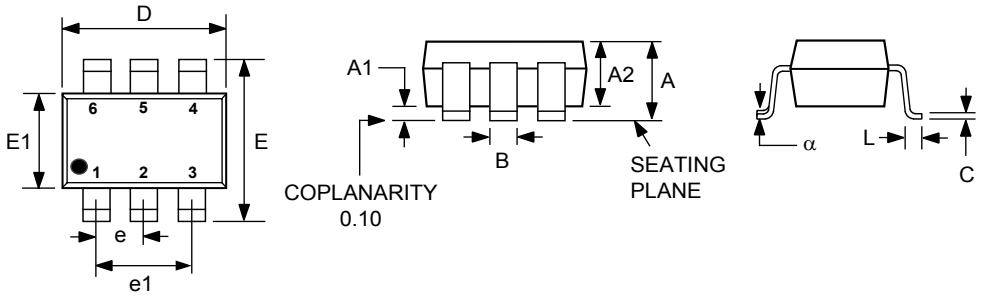
The Z_{VIN} is an iW3627 internal resistor connected from V_{IN_A} to ground (12.5kΩ typical, see Fig 8.1). The R_{IN} is the external resistor connected from the V_{IN} pin to a rectified line. The V_{BUS} is the rectified line voltage (Refer to Figure 3.1).

After the initial OTP check and configuration, the control logic waits for about 500µs before starting the input voltage brown-out check. Once the V_{IN_A} is higher than the V_{BRN_IN}, the iW3627 begins a soft-start function. The iW3627 continues to monitor line voltage through the V_{IN} pin afterwards; if the V_{IN_A} is lower than the V_{BRN_OUT} for several consecutive line cycles, the brown-out fault is triggered and the iW3627 shuts down. When the BRP occurs, the IC keeps biased to discharge V_{CC} supply. When The V_{CC} drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting start-up until the fault condition is removed.

It is recommended to add a 1nF~2.2nF ceramic capacitor between the V_{IN} pin and IC ground for decoupling purpose.

10.0 Physical Dimensions

6-Lead SOT Package



Symbol	Millimeters	
	MIN	MAX
A	-	1.45
A1	0.00	0.15
A2	0.90	1.30
B	0.30	0.50
C	0.08	0.22
D	2.90 BSC	
E	2.80 BSC	
E1	1.60 BSC	
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
α	0°	8°

Compliant to JEDEC Standard MO-178AB

Controlling dimensions are in millimeters

This package is RoHS compliant and Halide free.

Soldering Temperature Resistance:
[a] Package is IPC/JEDEC Std 020D Moisture Sensitivity Level 1
[b] Package exceeds JEDEC Std No. 22-A111 for Solder Immersion Resistance; packages can withstand 10 s immersion < 260ºC

Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.25 mm per side.

The package top may be smaller than the package bottom. Dimensions D and E1 are are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs and interlead flash, but including any mismatch between top and bottom of the plastic body.

11.0 Ordering Information

Part Number	Options	Package	Description
iW3627-00	0.16V CS/F_{MIN} clamp, 64Ω pull-up resistor	SOT-23	Tape & Reel[1]
iW3627-01	0.20V CS/F_{MIN} clamp, 64Ω pull-up resistor	SOT-23	Tape & Reel[1]
iW3627-02	0.16V CS/F_{MIN} clamp, 16Ω pull-up resistor	SOT-23	Tape & Reel[1]
iW3627-03	0.20V CS/F_{MIN} clamp, 16Ω pull-up resistor	SOT-23	Tape & Reel[1]

Note 1: Tape & Reel packing quantity is 3,000/reel. Minimum ordering quantity is 3,000.

Off-Line Digital Constant-Voltage LED Driver with Power Factor Correction

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